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NONLINEAR CIRCUIT ANALYSIS PROGRAM (NCAP) DOCUMENTATION
Engineering Manual

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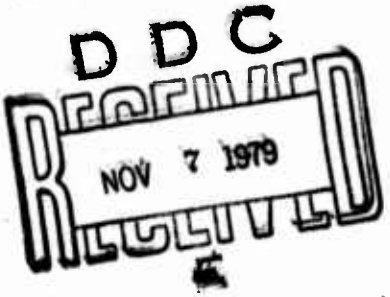

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The Nonlinear Circuit Analysis Program (NCAP) is a circuit analysis code which uses the Volterra approach to solve for the transfer functions and node voltages of nonlinear circuits. To increase the transportability, the code was written in ANSI FORTRAN. The code was revised and documented in a joint effort using both in-house and contracted manpower. This documentation is a result of that effort. The documentation is made up of three volumes: the Engineering Manual, the User's Manual, and the Programmer's Manual. (Cont'd)

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The Engineering Manual, Volume I, contains the introduction to the documentation, a description of the theory upon which NCAP is based, and the procedure for obtaining the input parameter data.

The User's Manual, Volume II, contains a detailed description of the NCAP input language. The description includes the input commands and data requirements. Examples are used throughout the manual to aid the user in understanding the input language.

The Programmer's Manual, Volume III, contains a subroutine by subroutine description of the code. Each subroutine has a trace map, functional flow diagram and narrative which will help the programmer to understand the structure of NCAP.

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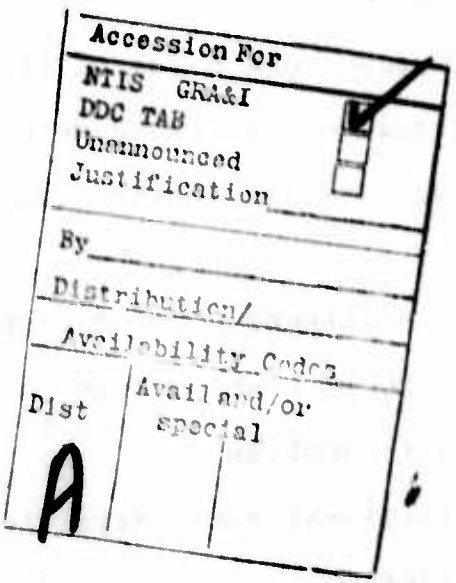

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SECTION 1

INTRODUCTION

SECTION 1: INTRODUCTION

1.1 General

NCAP is an acronym for the Rome Air Development Center's Nonlinear Circuit Analysis Program. It is a user-oriented computer code for determining the nonlinear transfer functions of electronic circuits. By utilizing a standard set of circuit elements, NCAP can analyze networks made up of interconnections of these elements.

NCAP is written in ANSI Standard FORTRAN and can analyze networks containing up to approximately 500 nodes. Sparse matrix routines are used to decrease core storage requirements and increase computational efficiency of the program.

Structurally, NCAP solves the nonlinear network problem by forming both the nodal admittance matrix (Y matrix) for the entire network, and the first-order generator (current-source) excitation vector, for all of the linear sources in the entire network. The generators can be located at any node in the network, and can have any desired frequency, amplitude and phase. Using Gaussian elimination with the admittance matrix and the current vector results in the first-order nodal voltage vector for the network, the elements of which are the first-order transfer functions at all nodes in the network at the given excitation frequency. When there is more than one generator at a given frequency, the first-order transfer function will be the

total transfer function due to the superposition of the generators since the first-order transfer function is a linear function. The higher-order transfer functions are solved iteratively, using techniques described in Volume I, Section II.

NCAP is relatively simple to employ. The user enters a description of the circuit to be analyzed. NCAP interprets the input statements, performs the nonlinear analysis, and outputs the results in printed form. There are several types of input statements which are needed to analyze a given circuit. The input statements define the topology of the circuit, the circuit element values, the linear and nonlinear devices used in the circuit, the circuit excitation and the order of the analysis, the desired output, the data modification and sweeping descriptions.

1.2 ORGANIZATION OF THE DOCUMENT

This document consists of three volumes. Volume I, the Engineering Manual, contains introductory remarks on the history of NCAP, a review of the Volterra analysis technique, a presentation of the circuit equations programmed in NCAP, and detailed discussions of the active NCAP circuit element models as well as experimental techniques for determining the model parameters. Volume II, the User's Manual, contains an operational introduction to the NCAP program and Volume III, the Programmer's Manual, contains narrative descriptions of the NCAP subroutines, functional flow diagrams depicting the general flow of logic through the program, and trace maps which identify the subroutine linkages.

1.3 BACKGROUND

The Rome Air Development Center (RADC) has been tasked with the development of analysis techniques for weapon system electromagnetic compatibility (EMC) assurance. This development effort is formally known as the Air Force Intrasystem Analysis Program (IAP). The IAP concept, initiated within the Air Force in the early 1970's, presently consists of a collection of computer-aided analysis routines for addressing various aspects of intrasystem EMC. The analysis routines range in applicability from an overall system (aircraft, satellite, etc.) level EMC model to detailed wire coupling and circuit analysis models (NCAP). The intent is to provide the EMC analyst and system designer with an assemblage of techniques for solving EMC problems which often present themselves in varying degrees of complexity. NCAP, under the general framework of the IAP, could be applied after a more coarse analysis has indicated a potential EMC problem at the circuit level. At this point NCAP could be used to examine in more detail, the nonlinear effects which are often encountered in practice and can severely degrade system performance. It can be shown that many important nonlinear interference effects such as desensitization, intermodulation, and cross modulation can be specified in terms of the nonlinear transfer functions, functions computed by NCAP. A knowledge of the magnitude of these effects could be very valuable in the early stages of system design.

1.4 APPROPRIATE CLASS OF PROBLEMS

NCAP is applicable to a specific class of nonlinear problems. Although considerable progress has been made in the development of analytical techniques, there is no general solution technique available for all classes of nonlinear problems. NCAP is devoted to the class of nonlinear problems known as "weakly nonlinear". The nonlinearities in this type of problem are characterized by gradual, rather than abrupt, variations. Weakly nonlinear systems encompass an extensive class of practical systems. They include small-signal mixers and square-law detectors as well as the large class of "quasi-linear" circuits. By quasi-linear, we mean those circuits designed to be linear, but in fact, exhibit nonlinear behavior over some region of operation. An example would be the amplification region of a transistor amplifier. Although designed to linearly amplify input signals, close inspection will show that this is not the case; and indeed, the output wave form is not an exact replica of the input. The extent of this "degradation" is often of serious concern and can limit amplifier, and consequently, system performance.

SECTION 2

THE NONLINEAR TRANSFER FUNCTION APPROACH

SECTION 2: THE NONLINEAR TRANSFER FUNCTION APPROACH

2.1 Introduction

The analysis of nonlinear systems is complicated by the fact that no single analytical tool is generally applicable. However, various approaches are available for specific classes of nonlinear systems. For the special case of weakly nonlinear systems the Volterra functional series, otherwise known as the nonlinear transfer function approach, has proven to be an effective analysis method.

Consider a weakly nonlinear circuit with input x(t) and output y(t). The nonlinear transfer function approach models the circuit as shown in Fig. 2.1. This model consists of the parallel combination of N blocks with each block having, as a common input, the circuit excitation x(t). The output of the nth block is denoted by $y_n(t)$; n=1,2,...,N. The total system response is obtained by summing the outputs of the individual blocks so as to yield

$$y(t) = y_1(t) + y_2(t) + \ldots + y_N(t) = \sum_{n=1}^{N} y_n(t). \quad (2.1\text{-}1)$$

The nth block, characterized by the nth-order nonlinear transfer function $H_n(f_1, f_2, \ldots, f_n)$, is of nth order in the sense that multiplication of the input x(t) by a constant A results in multiplication of the output $y_n(t)$ by the constant A^n.

Thus, the nonlinear transfer function approach represents the output of a weakly nonlinear system as a sum of N individual

responses. The linear portion of the circuit, characterized by the conventional linear transfer function $H_1(f_1)$, generates the first-order component of the response. The quadratic portion of the circuit, characterized by $H_2(f_1,f_2)$, generates the second-order component of the response. Additional responses are generated in a similar manner. Blocks above Nth order are not included in the model because it is assumed they contribute negligibly to the output.

A weakly nonlinear system is completely characterized by its nonlinear transfer functions. Once these are known, the system output can be determined for any given input. This is analogous to the case of linear systems where knowledge of the linear transfer function is sufficient to completely specify the input-output relation.

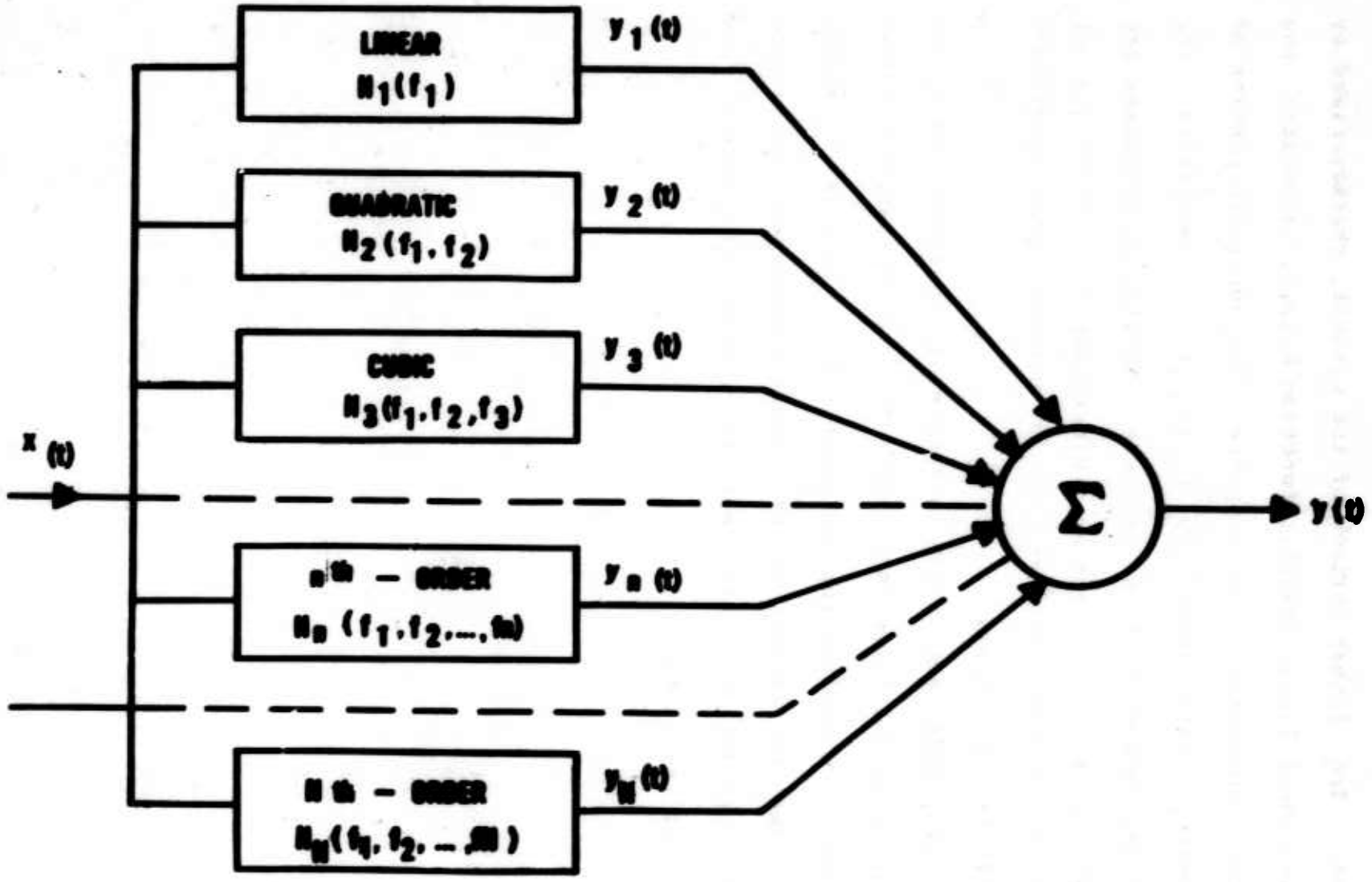

Fig. 2.1 Nonlinear transfer function model of a weakly nonlinear circuit.

2.2 Sinusoidal Steady-State Response of Weakly Nonlinear Systems

The sinusoidal steady-state response of weakly nonlinear systems is considered in this section. Let the input in Fig. 2.1 consist of the Q sinusoidal tones given by

$$x(t) = \sum_{q=1}^{Q} |X_q| \cos(2\pi f_q t + \theta_q) \qquad (2.2\text{-}1)$$

where the frequency, amplitude, and phase of the qth tone are denoted by f_q, $|X_q|$, and θ_q, respectively. In order to express (2.2-1) as a sum of complex exponentials, the complex amplitude of the qth tone is defined to be

$$X_q = |X_q| \exp[j\theta_q]. \qquad (2.2\text{-}2)$$

The input can then be expressed as

$$x(t) = \frac{1}{2} \sum_{q=-Q}^{Q} X_q \exp[j2\pi f_q t] \qquad (2.2\text{-}3)$$

where it is understood that

$$f_{-q} = -f_q \;, \quad X_{-q} = X_q^* \;, \quad X_0 = 0. \qquad (2.2\text{-}4)$$

In (2.2-4) the asterisk denotes complex conjugate. Whereas (2.2-1) involves only positive input frequencies, (2.2-3) suggests an interpretation whereby both positive and negative frequencies are contained in the input.

It is well known that the response of a system to a sum of sinusoids is a sum of sinusoids whether the system be linear or nonlinear. However, whereas the response frequencies of a linear system are identical to the input frequencies, new frequencies not present in the input are generated in the response of a nonlinear system. With reference to (2.2-3), the frequency content of x(t) consists of the 2Q frequencies $-f_Q, -f_{Q-1}, \ldots, -f_1, f_1, \ldots, f_{Q-1}, f_Q$. The output of the weakly nonlinear circuit of Fig. 2.1 contains frequencies of the form

$$m_{-Q}f_{-Q} + \ldots + m_{-1}f_{-1} + m_1 f_1 + \ldots + m_Q f_Q$$
$$= (m_1 - m_{-1})f_1 + \ldots + (m_Q - m_{-Q})f_Q \qquad (2.2\text{-}5)$$

where the coefficients m_k, $k=-Q,\ldots,-1,1,\ldots,Q$ are nonnegative integers. For a specific output frequency contained in the nth - order portion of the response $y_n(t)$, it is required that

$$m_{-Q} + \ldots + m_{-1} + m_1 + \ldots + m_Q = n. \qquad (2.2\text{-}6)$$

In general, the frequencies of $y_n(t)$ are generated by all possible choices of the nonnegative coefficients m_k such that the constraint given by (2.2-6) is satisfied.

Each separate choice of the coefficients m_k in (2.2-5) results in a different frequency mix. To characterize the various frequency mixes, it is convenient to introduce the frequency mix vector

$$\underline{m} = \{m_{-Q}, \ldots, m_{-1}, m_1, \ldots, m_Q\}. \qquad (2.2\text{-}7)$$

For example, with two sinusoidal inputs, Q=2 and $\underline{m}=\{m_{-2},m_{-1},m_1,m_2\}$. The vectors {1,0,1,0} {1,1,1,0}, and {0,0,0,2} then correspond to the frequency mixes $(-f_2+f_1)$, $(-f_2-f_1+f_1)$, and $(2f_2)$, respectively.

When the input x(t) consists of Q sinusoidal components, the number of distinct frequency mix vectors $\underline{m}$ associated with $y_n(t)$ is given by

$$M = \frac{(2Q + n - 1)!}{n!\ (2Q - 1)!} \quad . \qquad (2.2\text{-}8)$$

For example, with Q=2 (i.e., two sinusoidal inputs), there are four distinct frequency mixes associated with $y_1(t)$, ten distinct frequency mixes associated with $y_2(t)$, and twenty distinct frequency mixes associated with $y_3(t)$. The various frequency mix vectors and the corresponding frequency mixes are tabulated in Table 1. Note that the elements of each vector sum to the order n. This sum is referred to as the order of the frequency mix. For example, {2,1,0,2} corresponds to a frequency mix of order 5.

Frequencies that result from a frequency mix are termed intermodulation frequencies. The same intermodulation frequency can be generated by several different frequency mixes. For example, the different frequency mixes represented by {0,1,0,2}, {1,1,0,3}, and {0,2,1,2} all generate the same intermodulation frequency $2f_2-f_1$. For clarity of discussion, frequency mixes, such as $(-f_2-f_1+3f_2)$, are enclosed in parentheses whereas

intermodulation frequencies, such as $2f_2-f_1$, are not.

TABLE 2.2-1

Realization of $\{m_{-2},m_{-1},m_1,m_2\}$ for n=1,2, and 3

$\{m_{-2},m_{-1},m_1,m_2\}$	Frequency Mix	$\{m_{-2},m_{-1},m_1,m_2\}$	Frequency Mix
n=1			
{1,0,0,0}	$(-f_2)$	{0,0,1,0}	(f_1)
{0,1,0,0}	$(-f_1)$	{0,0,0,1}	(f_2)
n=2			
{1,1,0,0}	$(-f_2-f_1)$	{0,0,1,1}	(f_1+f_2)
{1,0,1,0}	$(-f_2+f_1)$	{0,1,0,1}	$(-f_1+f_2)$
{1,0,0,1}	$(-f_2+f_2)$	{0,1,1,0}	$(-f_1+f_1)$
{2,0,0,0}	$(-2f_2)$	{0,0,0,2}	$(2f_2)$
{0,2,0,0}	$(-2f_1)$	{0,0,2,0}	$(2f_1)$
n=3			
{1,1,1,0}	$(-f_2-f_1+f_1)$	{0,1,1,1}	$(-f_1+f_1+f_2)$
{1,1.0,1}	$(-f_2-f_1+f_2)$	{1,0,1,1}	$(-f_2+f_1+f_2)$
{2,1,0,0}	$(-2f_2-f_1)$	{0,0,1,2}	(f_1+2f_2)
{0,2,1,0}	$(-2f_1+f_1)$	{0,1,2,0}	$(-f_1+2f_1)$
{1,2,0,0}	$(-f_2-2f_1)$	{0.0,2,1}	$(2f_1+f_2)$
{2,0,0,1}	$(-2f_2+f_2)$	{1,0,0.2}	$(-f_2+2f_2)$
{2,0,1,0}	$(-2f_2+f_1)$	{0,1,0,2}	$(-f_1+2f_2)$
{0,2,0,1}	$(-2f_1+f_2)$	{1,0,2,0}	$(-f_2+2f_1)$
{3,0,0,0}	$(-3f_2)$	{0,0,0,3}	$(3f_2)$
{0,3,0,0}	$(-3f_1)$	{0,0,3,0}	$(3f_1)$

From (2.2-8) it is obvious that M, the number of distinct frequency mix vectors associated with $y_n(t)$, becomes large even for moderate values of Q and n. Fortunately, in most applications it is not necessary to evaluate all of the M resulting responses. In general, we are interested in only those frequency mixes which generate intermodulation frequencies that fall close to or within a system's pass band. Components that fall out of band are strongly attenuated and are not usually cause for concern. For example, consider a system tuned to 50 MHz with a 1 MHz bandwidth. Assume the input to consist of two out-of-band sinusoidal tones at f_1=46MHz and f_2=48MHz. The frequency mix vectors associated with $y_1(t)$, $y_2(t)$, and $y_3(t)$ are listed in Table 1. For the specified values of f_1 and f_2 intermodulation frequencies in $y_1(t)$, arranged in numerically increasing order, are -48, -46, 46, and 48 MHz. All of these are out of band and need not be considered. Similarly, the intermodulation frequencies in $y_2(t)$ are -96, -94, -92, -2, 0, 2, 92, 94 and 96 MHz. These also fall outside of the system pass band and need not be considered. Finally, the intermodulation frequencies in $y_3(t)$ are -144, -142, -140, -138, -50, -48, -46, -44, 44, 46, 48, 50, 138, 140, 142, and 144 MHz. Of these 16 intermodulation frequencies only those at -50 and 50 MHz fall in band. Hence, it is necessary to consider only the two responses of $y_3(t)$ associated with the frequency mix vectors {2,0,1,0} and {0,1,0,2}.

The next step is to evaluate the responses corresponding to the frequency mixes of interest. The nth-order transfer function

$H_n(f_1,\ldots,f_n)$ plays a significant role in determining the amplitudes and phases of the sinusoidal components in the nth-order portion of the response $y_n(t)$. In particular, an nth-order frequency mix characterized by the frequency mix vector $\underline{m}$ generates the response

$$y_n(t;\underline{m}) = |Y_{\underline{m}}| \cos[2\pi f_{\underline{m}} t + \phi_{\underline{m}}] \quad . \tag{2.2-9}$$

From (2.2-5) the response frequency is the intermodulation frequency

$$f_{\underline{m}} = (m_1 - m_{-1})f_1 + \ldots + (m_Q - m_{-Q})f_Q \quad . \tag{2.2-10}$$

The response amplitude depends upon the input amplitudes as well as the magnitude of the appropriate nonlinear transfer function. Specifically,

$$|Y_{\underline{m}}| = C_{\underline{m}} \frac{(n!)}{(m_{-Q}!)\ \ldots (m_{-1}!)\ (m_1!)\ \ldots\ (m_Q!)} \cdot |X_1|^{(m_1 + m_{-1})} \ldots |X_Q|^{(m_Q + m_{-Q})} \cdot |H_n(\underbrace{f_{-Q},\ldots,f_{-Q}}_{m_{-Q}},\ldots,\underbrace{f_{-1},\ldots,f_{-1}}_{m_{-1}},\underbrace{f_1,\ldots,f_1}_{m_1},\ldots,\underbrace{f_Q,\ldots,f_Q}_{m_Q})| \cdot \tag{2.2-11}$$

where

$$C_{\underline{m}} = \begin{cases} 2^{1-n} & , \quad f_{\underline{m}} \neq 0 \\ 2^{-n} & , \quad f_{\underline{m}} = 0 \quad . \end{cases} \tag{2.2-12}$$

Observe that the value of the constant $C_{\underline{m}}$ depends upon whether or not the intermodulation frequency is zero. The exponents associated with the input amplitudes are specified by the entries of the frequency mix vector. The frequency mix vector also determines the n arguments of the nonlinear transfer function. Specifically, the frequency f_k is used as an argument m_k times· k=-Q,...,-1,1,...,Q. The total number of arguments is n because of the constraint in (2.2-6). The order in which the n arguments appear is actually unimportant because the nonlinear transfer functions are symmetrical in their arguments. For example,

$$H_3(f_1,f_2,f_3) = H_3(f_1,f_3,f_2) = H_3(f_2,f_1,f_3) = H_3(f_2,f_3,f_1)$$
$$= H_3(f_3,f_1,f_2) = H_3(f_3,f_2,f_1) \qquad (2.2\text{-}13)$$

Finally, the response phase angle is a function of the input phase angles plus the phase angle of the nonlinear transfer function. In particular,

$$\phi_{\underline{m}} = \theta_{\underline{m}} + \psi_{\underline{m}} \qquad (2.2\text{-}14)$$

where

$$\theta_{\underline{m}} = (m_1 - m_{-1})\theta_1 + \ldots + (m_Q - m_{-Q})\theta_Q,$$
$$\psi_{\underline{m}} = \underline{/H_n(f_{-Q},\ldots,f_{-Q},\ldots,f_{-1},\ldots,f_{-1},f_1,\ldots,f_1,\ldots,f_Q,\ldots,f_Q)} \qquad (2.2\text{-}15)$$

Note that the manner in which the input phase angles combine in

(2.2-15) is identical to the way in which the input frequencies combine in (2.2-10). Also, the nth-order transfer function in (2.2-15) is the same as that in (2.2-11).

For a specific frequency mix vector, $y_n(t;\underline{m})$ is readily evaluated by straightforward application of (2.2-9) through (2.2-15). For example, consider the second-order frequency mixes characterized by the vectors {0,0,0,2}, {0,0,1,1}, and {1,0,0,1}. The corresponding second-order responses are

$$y_2(t;\{0,0,0,2\}) = \tfrac{1}{2}\,|X_2|^2\,|H_2(f_2,f_2)|\cos[2\pi(2f_2)t + 2\theta_2 + \psi_{\{0,0,0,2\}}]$$

$$y_2(t;\{0,0,1,1\}) = |X_1|\,|X_2|\,|H_2(f_1,f_2)|\cos[2\pi(f_1+f_2)t + \theta_1 + \theta_2 + \psi_{\{0,0,1,1\}}]$$

$$y_2(t;\{1,0,0,1\}) = \tfrac{1}{2}\,|X_2|^2\,|H_2(f_2,-f_2)|\cos[\psi_{\{1,0,0,1\}}] \qquad (2.2\text{-}16)$$

In general, nonlinear transfer functions associated with zero intermodulation frequencies are real quantities. Hence, $\psi_{\{1,0,0,1\}}$ is either zero degrees or 180 degrees.

It is important to remember that the same intermodulation frequency can be generated by several different frequency mixes. Consequently, it is necessary to sum the responses of all the frequency mixes which generate a particular intermodulation frequency. The total response at frequency f is denoted by y(t;f). To illustrate this point, consider a weakly nonlinear circuit for which the highest order response is of fifth order (i.e., N=5 in Fig. 2.1), Let the input consist of two sinusoids at frequencies f_1 and f_2 (i.e., Q=2). The output contains an intermodulation frequency at $2f_2-f_1$ which is generated by the three frequency mixes characterized by the frequency mix vectors

{0,1,0,2}, {1,1,0,3}, and {0,2,1,2} . Hence, the total response at $2f_2-f_1$ is given by

$$
\begin{aligned}
y(t;2f_2 - f_1) &= y_3(t;\{0,1,0,2\}) + y_5(t;\{1,1,0,3\}) + y_5(t;\{0,2,1,2\}) \\
&= \frac{3}{4} \; |X_1| \; |X_2|^2 \; |H_3(-f_1,f_2,f_2)| \\
&\quad \cos[2\pi(2f_2-f_1)t + 2\theta_2 - \theta_1 + \psi_{\{0,1,0,2\}}] \\
&\quad + \frac{5}{4} \; |X_1| \; |X_2|^4 \; |H_5(-f_2,-f_1,f_2,f_2,f_2)| \\
&\quad \cos[2\pi(2f_2 - f_1)t + 2\theta_2 - \theta_1 + \psi_{\{1,1,0,3\}}] \\
&\quad + \frac{15}{8} \; |X_1|^3 \; |X_2|^2 \; |H_5(-f_1,-f_1,f_1,f_2,f_2)| \\
&\quad \cos[2\pi(2f_2 - f_1)t + 2\theta_2 - \theta_1 + \psi_{\{0,2,1,2\}}]
\end{aligned}
\tag{2.2-17}
$$

In general, the angles $\psi_{\{0,1,0,2\}}$, $\psi_{\{1,1,0,3\}}$, and $\psi_{\{0,2,1,2\}}$ are not equal. The various terms in (2.2-17) combine as shown in the phase diagram of Fig. 2.2. Note that both magnitude and phase angles of the nonlinear transfer functions are important in determining the total response at a particular intermodulation frequency. For very small values of $|X_1|$ and $|X_2|$, the response is dominated by the third-order term and the fifth-order terms may be ignored. However, the fifth-order terms become significant as the input tones are increased in amplitude. Finally, for very large values of $|X_1|$ and $|X_2|$, the response is dominated by the fifth-order terms.

Having demonstrated the role played by the nonlinear transfer functions in the sinusoidal steady-state response of weakly nonlinear circuits, the procedure used by NCAP to determine the nonlinear transfer functions is discussed next.

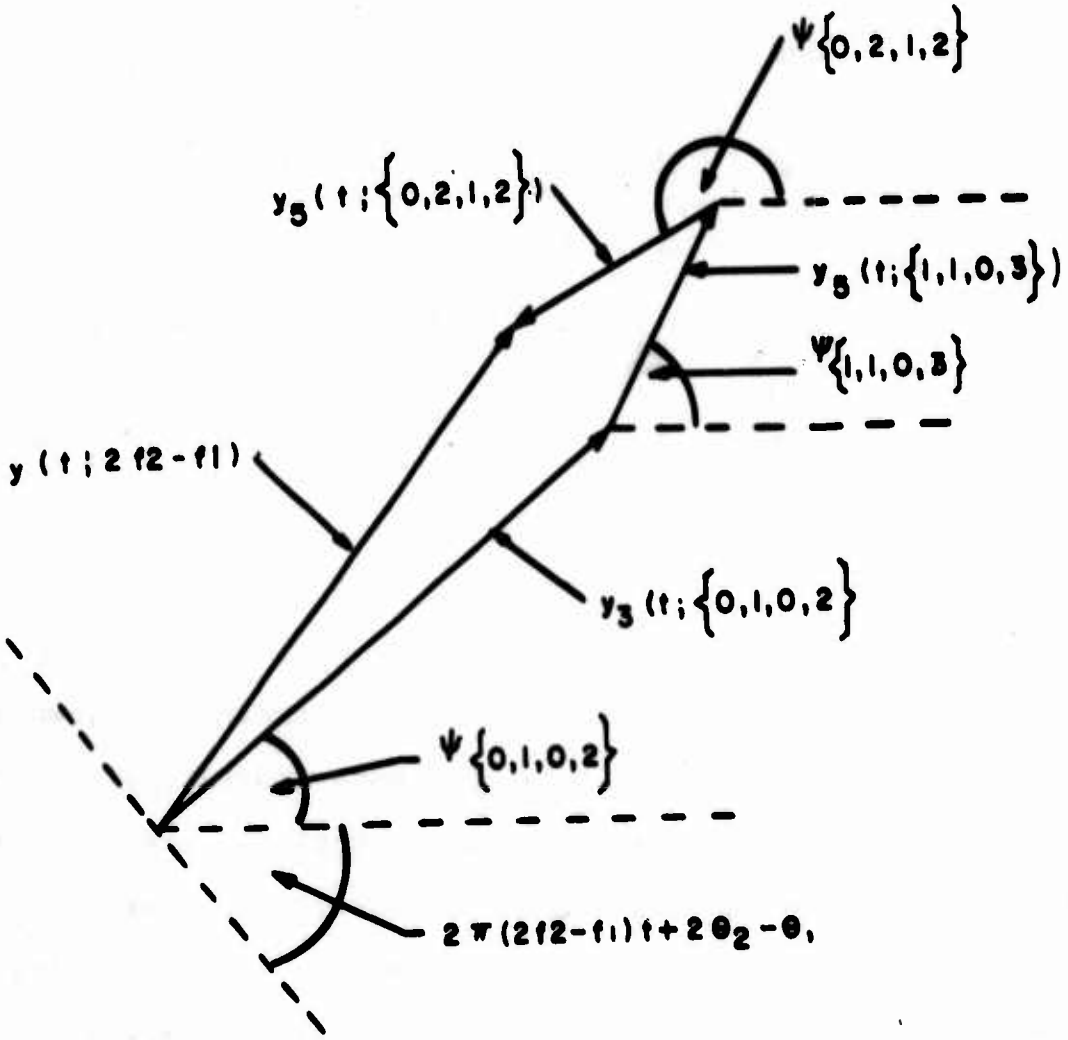

Fig. 2.2 Phasor diagram illustrating total response at the intermodulation frequency $2f_2-f_1$.

2.3 NCAP Procedure for Determination of $H(f_1, f_2, \ldots, f_n)$

The basic nonlinear circuit elements found in NCAP are the nonlinear resistor, nonlinear capacitor, nonlinear inductor, and nonlinear controlled sources. These are adequate for modeling the nonlinearities of most electronic devices such as diodes, vacuum tubes, transistors, integrated circuits, etc. In weakly nonlinear circuits electronic devices are typically operated over a localized region of their characteristics. Therefore, it is possible to expand the nonlinearities in power series about the quiescent operating point in terms of incremental variables. The series representations of the basic nonlinear circuit elements are presented next.

Let $e_r(t)$ and $i_r(t)$ denote the incremental voltage and current associated with a nonlinear resistor. The incremental current through the resistor may be expressed as

$$i_r(t) = \sum_{k=1}^{\infty} g_k [e_r(t)]^k \quad . \tag{2.3-1}$$

Note that g_1 is the conductance of the linear resistor normally included in a linear incremental equivalent circuit. Similarly, let $e_c(t)$ and $i_c(t)$ denote the incremental voltage and current associated with a nonlinear capacitor. The incremental current through the capacitor is given by

$$i_c(t) = \sum_{k=0}^{\infty} C_k [e_c(t)]^k \frac{de_c(t)}{dt} \tag{2.3-2}$$

The term corresponding to k=0 is in the usual form for a linear capacitor. Hence, C_o is the capacitance of the linear capacitor to be inserted into a linear incremental equivalent circuit." For a nonlinear inductor the series representation of the current is

$$i_\ell(t) = \sum_{k=1}^{\infty} \Gamma_k \left[\int_{-\infty}^{t} e_\ell(z)\, dz\right]^k \qquad (2.3\text{-}3)$$

where $e_\ell(t)$ and $i_\ell(t)$ are the incremental variables associated with the inductor. Γ_1 is the reciprocal inductance of the linear inductor that would be placed in a linear incremental equivalent circuit.

The final nonlinear circuit elements to be discussed are the nonlinear controlled sources. These occur frequently in electronic device models and are two-terminal elements whose terminal voltage or current is a nonlinear function of either the control voltage e_x or the control current i_x from some other part of the circuit. If the control variable pertains to a particular circuit element X, this element is called the controlling element. The series representations for the four types of nonlinear controlled sources are:

a) Voltage - controlled voltage source

$$e_{cs}(t) = \sum_{k=1}^{\infty} \mu_k [e_x(t)]^k , \qquad (2.3\text{-}4)$$

b) Current - controlled voltage source

$$e_{cs}(t) = \sum_{k=1}^{\infty} r_{ks}[i_x(t)]^k \quad , \qquad (2.3\text{-}5)$$

c) Voltage - controlled current source

$$i_{cs}(t) = \sum_{k=1}^{\infty} g_{ks}[e_x(t)]^k \quad , \qquad (2.3\text{-}6)$$

d) Current - controlled current source

$$i_{cs}(t) = \sum_{k=1}^{\infty} \alpha_k[i_x(t)]^k \quad . \qquad (2.3\text{-}7)$$

The linear term in each expansion defines the linear controlled source to be used in linear incremental equivalent circuits. The linear coefficients μ_1, r_{1s}, g_{1s}, and α_1, are referred to as the voltage amplification factor, the mutual resistance, the mutual conductance, and the current amplification factor, respectively.

The procedure employed by NCAP to solve for the nonlinear transfer functions makes use of nodal analysis. This approach was chosen, as opposed to loop analysis, because electronic circuits tend to have many fewer nodes than loops. Assume the circuit to be analyzed contains K+1 nodes. One of the nodes, usually the ground connection, is assigned to be the reference or datum node. Node-to-datum voltages are then defined for each of the remaining K nodes. Let $v^j(t)$ denote the node-to-datum voltage for node j. j=1,2,...K. (A superscript is used to avoid confusion with subscripts which are reserved for the designation

of order.) The nth-order transfer function at the jth node is denoted by $H_n^j(f_1,\ldots,f_n)$. Hence, the jth node has associated with it a set of nonlinear transfer functions of order 1 to N. The excitation is assumed to be a voltage source $v_g(t)$ with generator impedance $z_g(f)$. For convenience of discussion, let the source be connected between node 1 and the reference node.

The first step in the procedure is to write Kirchhoff's current law at each of the K nodes, other than the reference node. The current through each nonlinear circuit element is then expressed in a power series where the series variables are node-to-datum voltages. The linear term in each series can be represented by a linear circuit element. These are lumped with the linear portion of the network to form the augmented linear network. In terms of the K Kirchhoff current law equations, this latter step is accomplished by rearranging the equations such that only terms linear in the node-to-datum voltages appear on the left hand side. The right side of the equations then contain only the source term and the nonlinear terms from the power series expansions of the nonlinear circuit elements.

The solution procedure is recursive in nature. The augmented linear circuit is first excited by allowing $v_g(t)$ to be the single complex exponential $\exp[\, j2\pi f_1 t\,]$. This permits determination of the linear transfer function. Then the sum of two complex exponentials, given by $v_g(t) = \exp[\, j2\pi f_1 t\,] + \exp[\, j2\pi f_2 t\,]$, is applied. This yields the second-order transfer function in terms of the linear transfer function. The procedure continues with one additional complex exponential being added to

the input at each step. Therefore, at step n, the input consists of the sum $v_g(t)=\exp[\,j2\pi f_1 t\,] + \ldots + \exp[j2\pi f_n t\,]$. The nth -order transfer function is then found to be constructed from all of the previously determined lower order nonlinear transfer functions.

Let the admittance matrix of the augmented linear network be denoted by $[Y(f)]$. Also, define the nth-order nonlinear transfer function vector to be

$$\underline{H}_n(f_1,\ldots,f_n) = \begin{bmatrix} H_n^1(f_1,\ldots,f_n) \\ H_n^2(f_1,\ldots,f_n) \\ \vdots \\ H_n^K(f_1,\ldots,f_n) \end{bmatrix} \qquad (2.3\text{-}8)$$

The first-order transfer functions for the various node-to-datum voltages are simply the conventional linear transfer functions and are obtained by solving the matrix equation

$$[\,Y(f_1)\,]\,\underline{H}_1(f_1) = \left[\,\frac{1}{Z_g(f_1)} \quad 0 \quad 0 \quad \ldots \quad 0\,\right]^T \qquad (2.3\text{-}9)$$

where T denotes the transpose operator.

The second-order nonlinear transfer functions are determined next and the procedure continues recursively for each of the higher transfer functions. In general, the nth-order transfer functions are solutions to the matrix equation

$$[\,Y(f_1 + \ldots + f_n)\,]\,\underline{H}_n(f_1,\ldots,f_n) = \underline{I}_n(f_1,\ldots,f_n) \qquad (2.3\text{-}10)$$

where the nth-order source vector, $\underline{I}_n(f_1,\ldots,f_n)$, is a function of the lower order nonlinear transfer functions. At each stage of the solution, note that it is the admittance matrix of the augmented linear network which is evaluated at the appropriate frequency and then inverted.

The jth entry in the nth-order source vector arises from the nth-order currents associated with the nonlinear circuit elements connected to node j. Evaluation of these entries becomes increasingly tedious as n grows in value. The situation is aided by means of a recursion relationship which has been developed for this purpose. The exact form of the relationship depends upon whether the nonlinearity is a zero-memory nonlinearity (i.e., a nonlinear resistor or a nonlinear controlled source), a capacitive nonlinearity, or an inductive nonlinearity. The zero-memory nonlinearity is discussed first.

Consider a zero-memory nonlinearity of the form

$$i(t) = \sum_{k=2}^{\infty} a_k [v^p(t)]^k \qquad (2.3\text{-}11)$$

where $v^p(t)$ denotes the node-to-datum voltage for node p. The linear term has been omitted in (2.3-11) because it is included with the augmented linear network. If the nonlinear circuit element is connected to node j, the jth entry of the nth-order source vector is given by

$$I_n^j(f_1,\ldots,f_n) = \overline{V_n^j(f_1,\ldots,f_n)} \qquad (2.3\text{-}12)$$

where the overbar is used to denote the arithmetic average of the n! terms generated by all possible permutations of the n frequencies. For example,

$$I_3^j(f_1,f_2,f_3) = \overline{V_3^j(f_1,f_2,f_3)} = \frac{1}{6}\left[V_3^j(f_1,f_2,f_3) + V_3^j(f_1,f_3,f_2)\right.$$
$$\left. + V_3^j(f_2,f_1,f_3) + V_3^j(f_2,f_3,f_1) + V_3^j(f_3,f_1,f_2) + V_3^j(f_3,f_2,f_1)\right] \qquad (2.3\text{-}13)$$

The quantity $V_n^j(f_1,\ldots,f_n)$ may be expressed as

$$V_n^j(f_1,\ldots,f_n) = \sum_{k=2}^{n} a_k \; H_{n,k}^p(f_1,\ldots,f_n) \qquad (2.3\text{-}14)$$

where a recursion relationship for $H_{n,k}^p(f_1,\ldots,f_n)$ is

$$H_{n,k}^p(f_1,\ldots,f_n) = \sum_{i=1}^{n-k+1} H_i^p(f_1,\ldots,f_i)\, H_{n-i,k-1}^p(f_{i+1},\ldots,f_n) \; . \qquad (2.3\text{-}15)$$

Recall that the ith-order transfer function at the pth node is denoted by $H_i^p(f_1,\ldots,f_i)$. $H_{n,k}^p(f_1,\ldots,f_n)$ has the properties that

$$H_{n,k}^p(f_1,\ldots,f_n) = \begin{cases} H_n^p(f_1,\ldots,f_n) & ; \; k=1 \\ 0 & ; \; k>n \; . \end{cases} \qquad (2.3\text{-}16)$$

Because of the permutations implied by the overbar in (2.3-12), the order in which the n frequencies are assigned to $H_i^p(\ )$ and $H_{n-i,\,k-1}^p(\ \ )$ in the sum of (2.3-15) is immaterial as long as each frequency appears once and only once. For the sake of consistency, let the frequencies be assigned consecutively beginning with the factors requiring the fewest arguments.

By way of example, the following results are obtained through application of (2.3-15) and (2.3-16):

$$H_{1,1}^p(f_1) = H_1^p(f_1)$$

$$H_{2,1}^p(f_1,f_2) = H_2^p(f_1,f_2)\ ,\ H_{2,2}^p(f_1,f_2) = H_1^p(f_1)\ H_1^p(f_2)$$

$$H_{3,1}^p(f_1,f_2,f_3) = H_3^p(f_1,f_2,f_3)\ ,\ H_{3,2}^p(f_1,f_2,f_3) = 2H_1^p(f_1)\ H_2^p(f_2,f_3)\ ,$$

$$H_{3,3}^p(f_1,f_2,f_3) = H_1^p(f_1)\ H_1^p(f_2)\ H_1^p(f_3)$$

$$H_{4,1}^p(f_1,f_2,f_3,f_4) = H_4^p(f_1,f_2,f_3,f_4)\ ,\ H_{4,2}^p(f_1,f_2,f_3,f_4) = [H_2^p(f_1,f_2)\ H_2^p(f_3,f_4)$$

$$+ 2H_1^p(f_1)\ H_3^p(f_2,f_3,f_4)]\ ,$$

$$H_{4,3}^p(f_1,f_2,f_3,f_4) = 3H_1^p(f_1)\ H_1^p(f_2)\ H_2^p(f_3,f_4)\ ,$$

$$H_{4,4}^p(f_1,f_2,f_3,f_4) = H_1^p(f_1)\ H_1^p(f_2)\ H_1^p(f_3)\ H_1^p(f_4)$$

(2.3-17)

From (2.3-12) and (2.3-14), it follows that the jth entries of the nth-order source vector for n=2,3, and 4 are

$$I_2^j(f_1,f_2) = a_2 \overline{H_1^p(f_1)\ H_1^p(f_2)}$$

$$I_3^j(f_1,f_2,f_3) = 2a_2 \overline{H_1^p(f_1)\ H_2^p(f_2,f_3)} + a_3 \overline{H_1^p(f_1)\ H_1^p(f_2)\ H_1^p(f_3)}$$

$$I_4^j(f_1,f_2,f_3,f_4) = a_2[\overline{H_2^p(f_1,f_2)\ H_2^p(f_3,f_4)} + 2\overline{H_1^p(f_1)\ H_3^p(f_2,f_3,f_4)}] \qquad (2.3\text{-}18)$$

$$+ 3a_3 \overline{H_1^p(f_1)\ H_1^p(f_2)\ H_2^p(f_3,f_4)} + a_4 \overline{H_1^p(f_1)\ H_1^p(f_2)\ H_1^p(f_3)\ H_1^p(f_4)}$$

Observe that the nth-order entry involves only nonlinear transfer functions of lower order.

A nonlinear capacitor is now assumed to be connected between nodes j and p. Let the nonlinear portion of the current through the capacitor be given by

$$i(t) = \sum_{k=1}^{\infty} C_k [v^{jp}(t)]^k \frac{dv^{jp}(t)}{dt} = \frac{d}{dt}\left\{ \sum_{k=2}^{\infty} \frac{C_{k-1}}{k} [v^{jp}(t)]^k \right\} \qquad (2.3\text{-}19)$$

where, as in (2.3-11), the linear term has been omitted. The voltage across the capacitor is

$$v^{jp}(t) = v^j(t) - v^p(t) \ . \qquad (2.3\text{-}20)$$

The jth entry in the nth-order source vector is given by (2.3-12). However, now

$$V_n^j(f_1,\ldots,f_n) = j2\pi(f_1 + \ldots + f_n) \sum_{k=2}^{n} \frac{C_{k-1}}{k} H_{n,k}^{jp}(f_1,\ldots,f_n) \qquad (2.3\text{-}21)$$

where

$$H_{n,k}^{jp}(f_1,\ldots,f_n) = H_{n,k}^{j}(f_1,\ldots,f_n) - H_{n,k}^{p}(f_1,\ldots,f_n) \ . \qquad (2.3\text{-}22)$$

The recursion relation in (2.3-15) may, once again, be used with the superscript p replaced by jp. For example, application of (2.3-12), (2.3-21), and (2.3-15) for n=3 results in

$$I_3^j(f_1,f_2,f_3) = j2\pi(f_1+f_2+f_3)\left[2\,\frac{C_1}{2}\,\overline{H_1^{jp}(f_1)\,H_2^{jp}(f_2,f_3)} + \frac{C_2}{3}\,\overline{H_1^{jp}(f_1)\,H_1^{jp}(f_2)\,H_1^{jp}(f_3)}\right] . \tag{2.3-23}$$

The differences between the expressions in (2.3-18) and (2.3-23) for $I_3^j(f_1,f_2,f_3)$ should be noted carefully.

Finally, assume a nonlinear inductor is connected between nodes j and p. The nonlinear portion of the current through the inductor is

$$i(t) = \sum_{k=2}^{\infty} \Gamma_k \left[\int_{-\infty}^{t} v^{jp}(z)\,dz\right]^k . \tag{2.3-24}$$

As with the zero-memory nonlinearity and the nonlinear capacitor, the jth entry in the nth-order source vector is given by (2.3-12). However, now

$$V_n^j(f_1,\ldots,f_n) = \sum_{k=2}^{n} \Gamma_k\, G_{n,k}^{jp}(f_1,\ldots,f_n) \tag{2.3-25}$$

where a recursive relationship for $G_{n,k}^{jp}(f_1,\ldots,f_n)$ is

$$G_{n,k}^{jp}(f_1,\ldots,f_n) = \sum_{i=1}^{n-k+1} \frac{H_i^{jp}(f_1,\ldots,f_i)}{j2\pi(f_1+\ldots+f_i)}\, G_{n-i,k-1}^{jp}(f_{i+1},\ldots,f_n) . \tag{2.3-26}$$

$G^{jp}_{n,k}(f_1,\ldots,f_n)$ has the properties that

$$G^{jp}_{n,k}(f_1,\ldots,f_n) = \begin{cases} \dfrac{H^{jp}_n(f_1,\ldots,f_n)}{j2\pi(f_1+\ldots+f_n)} & ; \quad k=1 \\ 0 & ; \quad k>n\ . \end{cases} \tag{2.3-27}$$

As with (2.3-15), let the n frequencies in the sum of (2.3-26) be assigned consecutively beginning with the factors requiring the fewest arguments.

As an illustration of (2.3-26) and (2.3-27), note that

$$G^{jp}_{1,1}(f_1) = \frac{H^{jp}_1(f_1)}{j2\pi f_1}$$

$$G^{jp}_{2,1}(f_1,f_2) = \frac{H^{jp}_2(f_1,f_2)}{j2\pi(f_1+f_2)} \quad , \quad G^{jp}_{2,2}(f_1,f_2) = \frac{H^{jp}_1(f_1)}{j2\pi f_1}\ \frac{H^{jp}_1(f_2)}{j2\pi f_2}$$

$$G^{jp}_{3,1}(f_1,f_2,f_3) = \frac{H^{jp}_3(f_1,f_2,f_3)}{j2\pi(f_1+f_2+f_3)} \quad , \quad G^{jp}_{3,2}(f_1,f_2,f_3) = 2\frac{H^{jp}_1(f_1)}{j2\pi f_1}$$

$$\frac{H^{jp}_2(f_2,f_3)}{j2\pi(f_2+f_3)} \quad , \quad G^{jp}_{3,3}(f_1,f_2,f_3) = \frac{H^{jp}_1(f_1)}{j2\pi f_1}\ \frac{H^{jp}_1(f_2)}{j2\pi f_2}\ \frac{H^{jp}_1(f_3)}{j2\pi f_3} \tag{2.3-28}$$

The jth entry in the nth-order source vector is obtained by a straightforward application of (2.3-12) and (2.3-25). For

example, with n=3

$$I_3^j(f_1,f_2,f_3) = 2\Gamma_2 \overline{\frac{H_1^{jp}(f_1)}{j2\pi f_1} \frac{H_2^{jp}(f_2,f_3)}{j2\pi(f_2+f_3)}} + \Gamma_3 \overline{\frac{H_1^{jp}(f_1)}{j2\pi f_1} \frac{H_1^{jp}(f_2)}{j2\pi f_2} \frac{H_1^{jp}(f_3)}{j2\pi f_3}} . \quad (2.3\text{-}29)$$

We see, therefore, that the entries for $\underline{I}_n(f_1,\ldots,f_n)$ are readily obtained. The key step in the procedure involves use of the recursion relations given by (2.3-15) and (2.3-26).

The procedure used by NCAP to determine the nonlinear transfer functions is now illustrated by means of an example. Consider the weakly nonlinear incremental circuit shown in Fig. 2.3.

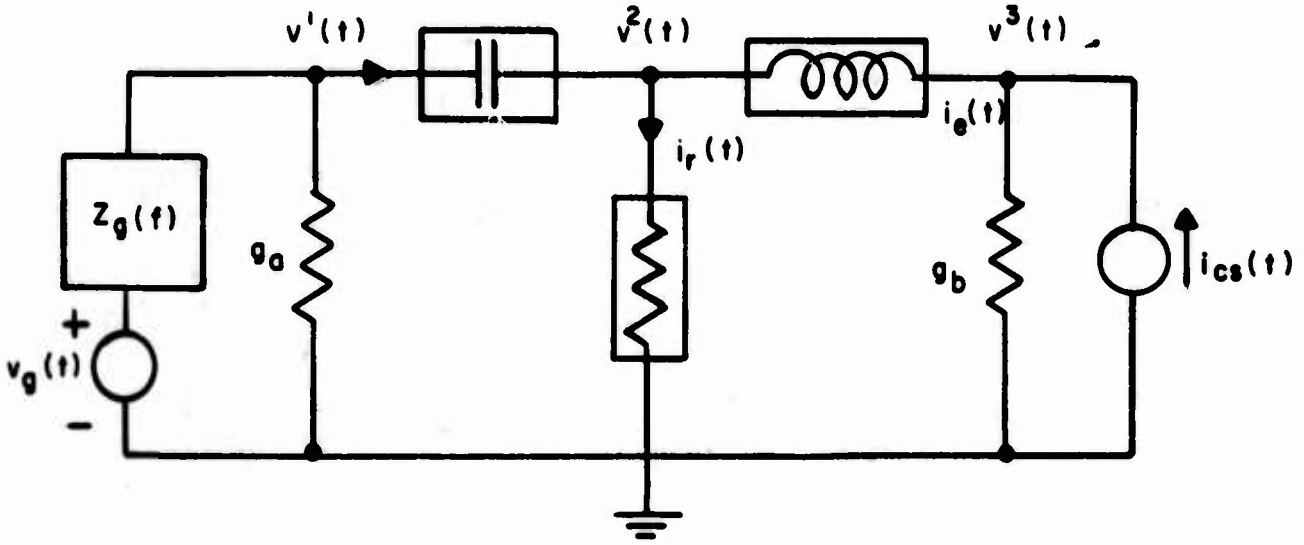

Fig. 2.3 Weakly nonlinear incremental circuit.

Enclosed in boxes, to distinguish them from linear elements, are a nonlinear capacitor, a nonlinear resistor, and a nonlinear inductor. The circuit also contains a nonlinear

Fig. 2.4 Equivalent circuit of nonlinear network shown in Fig. 2.3

voltage-controlled current source which is designated by $i_{cs}(t)$. The series expansions for the incremental currents through the nonlinear elements are

$$i_c(t) = \sum_{k=0}^{\infty} C_k[v^1(t) - v^2(t)]^k \cdot \frac{d[v^1(t) - v^2(t)]}{dt}$$

$$i_r(t) = \sum_{k=1}^{\infty} g_k[v^2(t)]^k \qquad (2.3\text{-}30)$$

$$i_\ell(t) = \sum_{k=1}^{\infty} \Gamma_k\{\int_{-\infty}^{t}[v^2(z) - v^3(z)]dz\}^k$$

$$i_{cs}(t) = \sum_{k=1}^{\infty} g_{ks}[v^1(t)]^k \quad .$$

For nodal analysis it is convenient to convert the independent voltage source $v_g(t)$ into a equivalent current source $i_N(t)$ by means of Norton's theorem. In addition, separating each power series in (2.3-30) into a linear term plus second-and higher-order terms, each nonlinear circuit element may be replaced by a linear circuit element in parallel with a nonlinear voltage-controlled current source. This is shown in Fig.4 for the circuit of Fig. 3. With this interpretation, the nonlinearities manifest themselves as controlled sources driving the augmented linear network. In Fig. 4

$$v^{12}(t) = v^1(t) - v^2(t) \qquad (2.3\text{-}31)$$

$$v^{23}(t) = v^2(t) - v^3(t) \, .$$

The admittance matrix of the augmented linear network is

$$[Y(f)] = \begin{bmatrix} \frac{1}{Z_g(f)} + g_a + j2\pi fC_0 & -j2\pi fC_0 & 0 \\ -j2\pi fC_0 & g_1 + j2\pi fC_0 + \frac{\Gamma_1}{j2\pi f} & -\frac{\Gamma_1}{j2\pi f} \\ -g_{ls} & -\frac{\Gamma_1}{j2\pi f} & g_b + \frac{\Gamma_1}{j2\pi f} \end{bmatrix}$$

(2.3-32)

The linear transfer functions are obtained by solving the matrix equation (2.3-9) while the higher order nonlinear transfer functions are solutions to the matrix equation (2.3-10). For n=2 and 3 the nth-order source vectors are given by (2.3-34) where

$$H_n^{12}(f_1,\ldots,f_n) = H_n^1(f_1,\ldots,f_n) - H_n^2(f_1,\ldots,f_n)$$

$$H_n^{23}(f_1,\ldots,f_n) = H_n^2(f_1,\ldots,f_n) - H_n^3(f_1,\ldots,f_n) \quad .$$

(2.3-33)

$$\underline{I}_2(\ell_1,\ell_2) = \begin{bmatrix} -j2\pi(\ell_1+\ell_2)\,\frac{C_1}{2}\quad \overline{H_1^{12}(\ell_1)\,H_1^{12}(\ell_2)} \\ \hline \{-g_2\ \overline{H_1^2(\ell_1)\,H_1^2(\ell_2)}\ -\Gamma_2\ \overline{\frac{H_1^{23}(\ell_1)}{j2\pi\ell_1}\ \frac{H_1^{23}(\ell_2)}{j2\pi\ell_2}}\ + j2\pi(\ell_1+\ell_2)\,\frac{C_1}{2} \\ \qquad\qquad \overline{H_1^{12}(\ell_1)\,H_1^{12}(\ell_2)}\ \} \\ \hline \{\Gamma_2\ \overline{\frac{H_1^{23}(\ell_1)}{j2\pi\ell_1}\ \frac{H_1^{23}(\ell_2)}{j2\pi\ell_2}}\ + g_{2s}\ \overline{H_1^1(\ell_1)\,H_1^1(\ell_2)}\ \} \end{bmatrix}$$

(2.3-34)

$$\underline{I}_3(\ell_1,\ell_2,\ell_3) = \begin{bmatrix} -j2\pi(\ell_1+\ell_2+\ell_3)\,[2\,\frac{C_1}{2}\,\overline{H_1^{12}(\ell_1)\,H_2^{12}(\ell_2,\ell_3)} + \frac{C_2}{3}\,\overline{H_1^{12}(\ell_1)\,H_1^{12}(\ell_2)\,H_1^{12}(\ell_3)}] \\ \hline \{-[2g_2\ \overline{H_1^2(\ell_1)\,H_2^2(\ell_2,\ell_3)}\ + g_3\ \overline{H_1^2(\ell_1)\,H_1^2(\ell_2)\,H_1^2(\ell_3)}] \\ -[2\Gamma_2\ \overline{\frac{H_1^{23}(\ell_1)}{j2\pi\ell_1}\ \frac{H_2^{23}(\ell_2,\ell_3)}{j2\pi(\ell_2+\ell_3)}}\ + \Gamma_3\ \overline{\frac{H_1^{23}(\ell_1)}{j2\pi\ell_1}\ \frac{H_1^{23}(\ell_2)}{j2\pi\ell_2}\ \frac{H_1^{23}(\ell_3)}{j2\pi\ell_3}}\ ] \\ + j2\pi(\ell_1+\ell_2+\ell_3)\,[2\,\frac{C_1}{2}\,\overline{H_1^{12}(\ell_1)\,H_2^{12}(\ell_2,\ell_3)} + \frac{C_2}{3}\,\overline{H_1^{12}(\ell_1)\,H_1^{12}(\ell_2)\,H_1^{12}(\ell_3)}]\} \\ \hline \{[2\Gamma_2\ \overline{\frac{H_1^{23}(\ell_1)}{j2\pi\ell_1}\ \frac{H_2^{23}(\ell_2,\ell_3)}{j2\pi(\ell_2+\ell_3)}}\ + \Gamma_3\ \overline{\frac{H_1^{23}(\ell_1)}{j2\pi\ell_1}\ \frac{H_1^{23}(\ell_2)}{j2\pi\ell_2}\ \frac{H_1^{23}(\ell_3)}{j2\pi\ell_3}}\ ] \\ +[\,2g_{2s}\ \overline{H_1^1(\ell_1)\,H_2^1(\ell_2,\ell_3)}\ + g_3\ \overline{H_1^1(\ell_1)\,H_1^1(\ell_2)\,H_1^1(\ell_3)}]\} \end{bmatrix}$$

Note that the jth entry in the Nth-order source vector consists of the sum of the contributions from the currents through each of the nonlinear circuit elements connected to node j. Also, the sign of each contribution is positive or negative depending upon whether the current flows into or out of the jth node.

2.4 Introduction to Electrical Device Modeling

The nonlinear analysis of an electronic circuit requires that each electronic device be replaced by an equivalent nonlinear circuit model. Most of the nonlinearities encountered in electronic devices are capable of being modeled by various combinations of nonlinear resistors, capacitors, inductors, and/or controlled sources. Several different circuit models are typically available for each device. Some are quite elaborate while others are relatively crude. Models which are highly accurate over large ranges of amplitude and frequency tend to be rather complicated and computationally inefficient. Furthermore, their complete description frequently entails a considerable amount of effort in order to obtain values for the large number of model parameters typically required. Less sophisticated models tend to be more efficient and easier to specify. However, since they arise by either neglecting or approximating various physical effects, they are limited in their usefulness. Nevertheless, simpler models can provide acceptable results in many situations.

NCAP provides stored nonlinear circuit models for the semiconductor diode, the bipolar junction transistor (BJT), the junction field-effect transistor (JFET), the vacuum-tube diode, the vacuum-tube triode, and the vacuum-tube pentode. Although the models used are not the most sophisticated, they have been shown to yield good results in practice. The circuit models are presented in the following sections. Where possible, analytical

expressions based upon the physics of the devices are given for the nonlinearities. Otherwise, empirical relations are utilized. The parameters associated with each device are defined. Finally, power series expansions of the incremental currents through the nonlinear circuit elements are presented.

The operation of electronic devices is usually depicted in terms of their static characteristics. These are plots relating a device's terminal voltages and currents as obtained from measurements performed under dc or very slowly varying conditions. Therefore, the static characteristics of actual devices do not include the effects of energy-storage elements and frequency-dependent parameters. Hence, the approach used to develop the incremental nonlinear equivalent circuit models was to first obtain a dc resistive equivalent circuit to model the static characteristics. Capacitors and inductors were then added at one or more strategic locations to account for the device's frequency behavior.

The region of operation for an electronic device is established by employing a dc biasing circuit which determines the dc or quiescent operating point. The application of additional signals then results in the device voltages and currents varying in some neighborhood about the operating point. It is important to distinguish between total, dc, and incremental variables. In this manual total variables are denoted by lower case symbols with upper case subscripts. For example, i_D and v_D represent the total current and voltage, respectively, of a diode. The dc value of a variable is denoted by an upper case

symbol with an upper case subscript. For a diode the dc current and voltage are denoted by I_D and V_D, respectively. Incremental variables are represented by lower case symbols with lower case subscripts and are defined to be the difference between the total and dc variables. For the diode the incremental current and voltage are given by

$$i_d = i_D - I_D$$

$$v_d = v_D - V_D \quad . \tag{2.4-1}$$

In the following sections both global circuit models, involving total variables, and incremental circuit models, involving incremental variables, are presented. In the schematic diagrams boxes are places around resistors and capacitors to denote nonlinear circuit elements.

2.5 Semiconductor Diode Model

A global model for the semiconductor diode is shown in Fig. 2.5.

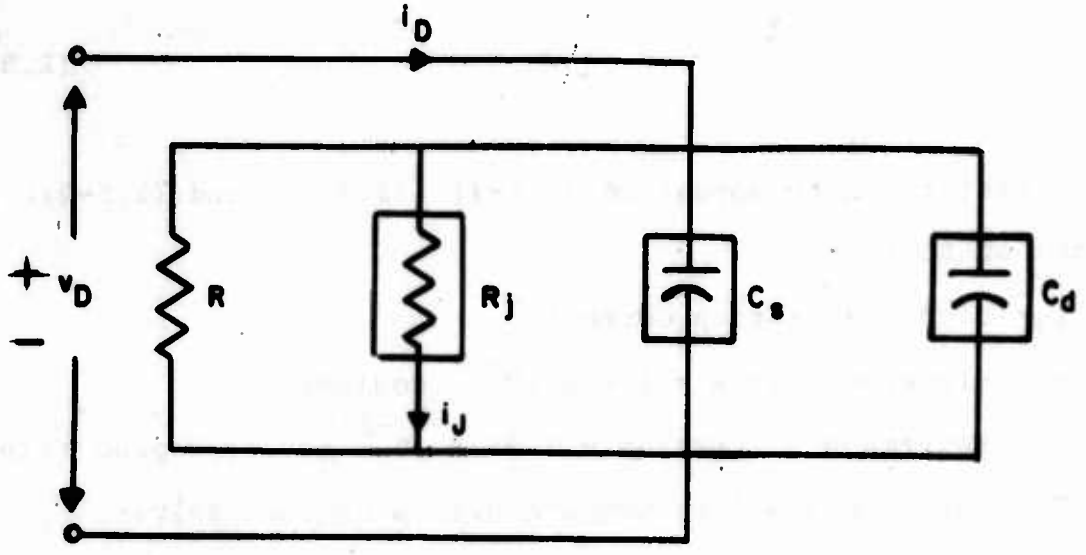

Fig. 2.5 Global model for semiconductor diode.

The four circuit elements in the global model are:

1) R, the junction leakage resistance.

2) R_j, the nonlinear resistor due to the diode junction. Its current-voltage relationship is given by

$$i_J = I_s \left[\exp\left(\frac{qv_D}{nkT}\right) - 1\right] . \qquad (2.5\text{-}1)$$

3) C_s, the nonlinear transition capacitance of the depletion layer, also known as the barrier capacitance or the space-charge capacitance. It is given by

$$C_s = K(-v_D)^{-\mu} , \quad v_D < 0 . \qquad (2.5\text{-}2)$$

4) C_d, the nonlinear diffusion capacitance whose value depends linearly on the junction current in accordance with the relation.

$$C_d = C_j' \; i_J \qquad (2.5\text{-}3)$$

The parameters which appear in (2.5-1), (2.5-2), and (2.5-3) are defined as follows:

I_s = diode saturation current,

q = electron charge = 1.6×10^{-19} coulombs,

k = Boltzmann's constant = 1.38×10^{-23} joules/degree Kelvin,

T = junction absolute temperature in degrees Kelvin,

n = diode nonideality factor,

K = transition capacitance at 1 volt reverse bias,

μ = junction grading constant,

C_j' = diffusion capacitance constant.

Near room temperature (T=290° K) kT/q is approximately 25 millivolts.

The global model may be simplified when the diode is either forward-or reverse-biased. We first consider forward-biased conditions for which $v_D > 0$. Since the forward resistance of R_j is then much smaller than that of R, negligible current flows through R and the leakage resistance may be ignored. Also, when the diode is forward biased, v_D is essentially constant relative to the junction current i_J. Therefore, the transition capacitance C_s may be treated as a constant which is denoted by C_j. A global model for the diode, in forward bias, is shown in

Fig. 2.6.

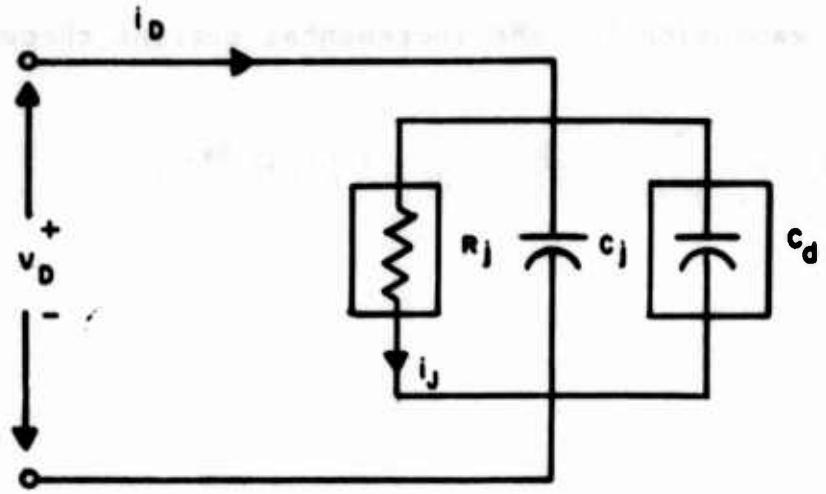

Fig. 2.6 Forward-biased global model for the semiconductor diode ($v_D > 0$).

The incremental current through R_j may be written as

$$i_j(t) = \sum_{k=1}^{\infty} g_k [v_d(t)]^k \qquad (2.5\text{-}4)$$

where

$$g_1 = \frac{nkT}{qI_D} \qquad (2.5\text{-}5)$$

and

$$g_k = \frac{1}{kI_D} g_1 \, g_{k-1} \, . \qquad (2.5\text{-}6)$$

Recall that I_D is the dc diode current. The linear incremental resistance of the diode, denoted by r_d, is the reciprocal of the

conductance g_1. Note that r_d is inversely proportional to I_D. The series expansion for the incremental current through C_d is

$$i_{cd}(t) = \sum_{k=0}^{\infty} \frac{C_{dk}}{k+1} \frac{d}{dt} \{ [v_d(t)]^{k+1} \} \qquad (2.5\text{-}7)$$

where

$$C_{d0} = C_j' I_D \qquad (2.5\text{-}8)$$

and

$$C_{dk} = C_j' g_k . \qquad (2.5\text{-}9)$$

The coefficients in the expansion for the diffusion capacitance are seen to be intimately related to those in the expansion for R_j. The forward-biased nonlinear incremental equivalent circuit for the semiconductor diode is shown in Fig. 2.7. Note that only

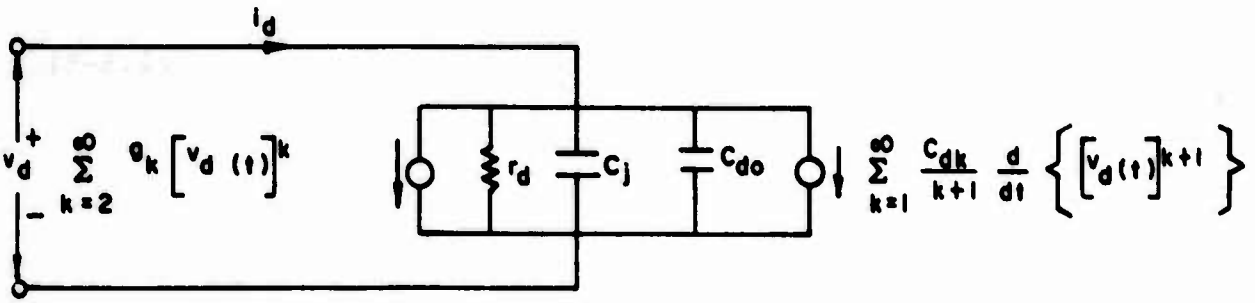

Fig. 2.7 Forward-biased nonlinear incremental equivalent circuit for semiconductor diode.

incremental variables appear in the model. Nevertheless r_d, C_{do}

and the series coefficients are functions of the quiescent operating point. The linear incremental equivalent circuit consists of r_d, C_j, and C_{do} all in parallel.

The diode is reverse biased when the diode voltage is negative. The junction current i_J and the diffusion capacitance C_d becomes negligibly small when $v_D < 0$. Therefore, under reverse-biased conditions, the diode global model is approximated by the circuit shown in Fig. 2.8. C_s is now the only nonlinear element contained in the model.

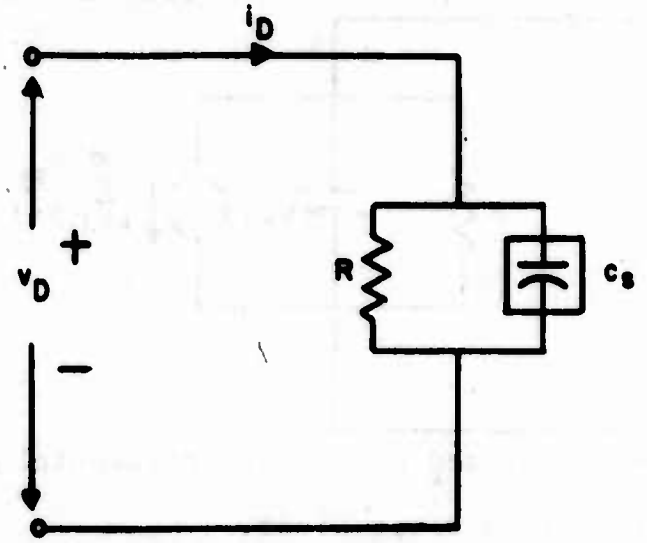

Fig. 2.8 Reverse-biased global model for the semiconductor diode ($v_D < 0$).

The incremental current through C_s is

$$i_{cs}(t) = \sum_{k=0}^{\infty} \frac{C_{sk}}{k+1} \frac{d}{dt} \{ [v_d(t)]^{k+1} \} \qquad (2.5\text{-}10)$$

where

$$C_{s0} = K (-V_D)^{-\mu} \qquad (2.5\text{-}11)$$

and

$$C_{sk} = \frac{(k + \mu - 1)}{k(-V_D)} C_{s(k-1)} \qquad (2.5\text{-}12)$$

V_D, of course, is the dc diode voltage. The reverse-biased nonlinear incremental equivalent circuit for the semiconductor diode is shown in Fig. 2.9. In practice, only a finite number of terms from the infinite sum are needed.

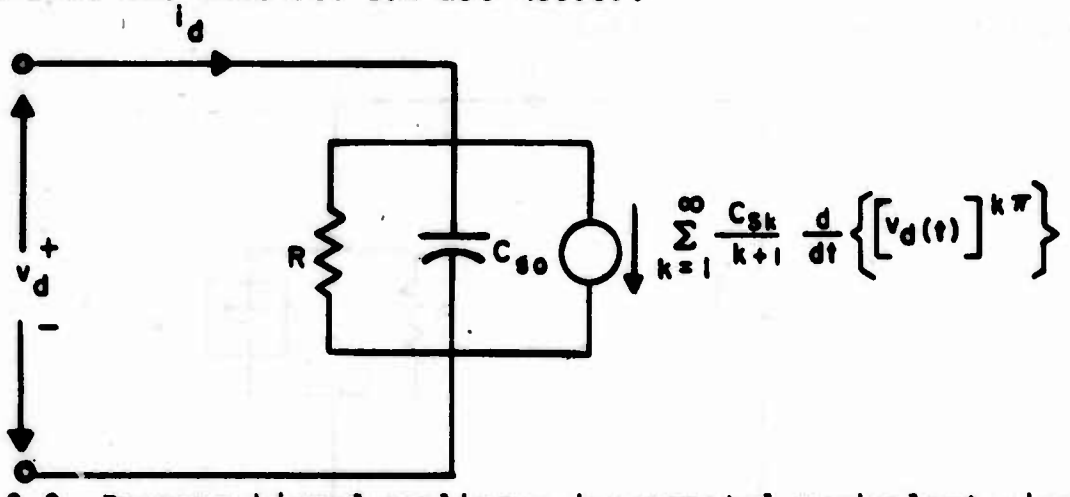

Fig. 2.9 Reverse-biased nonlinear incremental equivalent circuit for semiconductor diode.

2.6 Bipolar Junction Transistor Model

Weakly nonlinear effects are of concern primarily when the transistor is used as an amplifier. Consequently, attention in this section is confined to applications where the transistor operates solely in the amplification region. A global model for the bipolar junction transistor in the amplification region is presented in Fig. 2.10. The terminals denoted by E, B, and C are referred to as the emitter, base, and collector, respectively. Loosely speaking, a bipolar junction transistor may be viewed as two p-n junctions coupled back-to-back. In the amplification region the emitter-base junction is forward biased and the collector-base junction is reverse biased. The model of Fig. 2.10 can also be used for a pnp transistor except that all variables are reversed in polarity.

The seven elements in the global model are:

1) r_b, the base bulk resistance

2) R_{je}, the nonlinear resistor due to the emitter-base junction. Its current-voltage relationship is given by

$$i_{JE} = I_s \left[\exp\left(\frac{qv_{JE}}{nkT}\right) - 1\right] \quad . \tag{2.6-1}$$

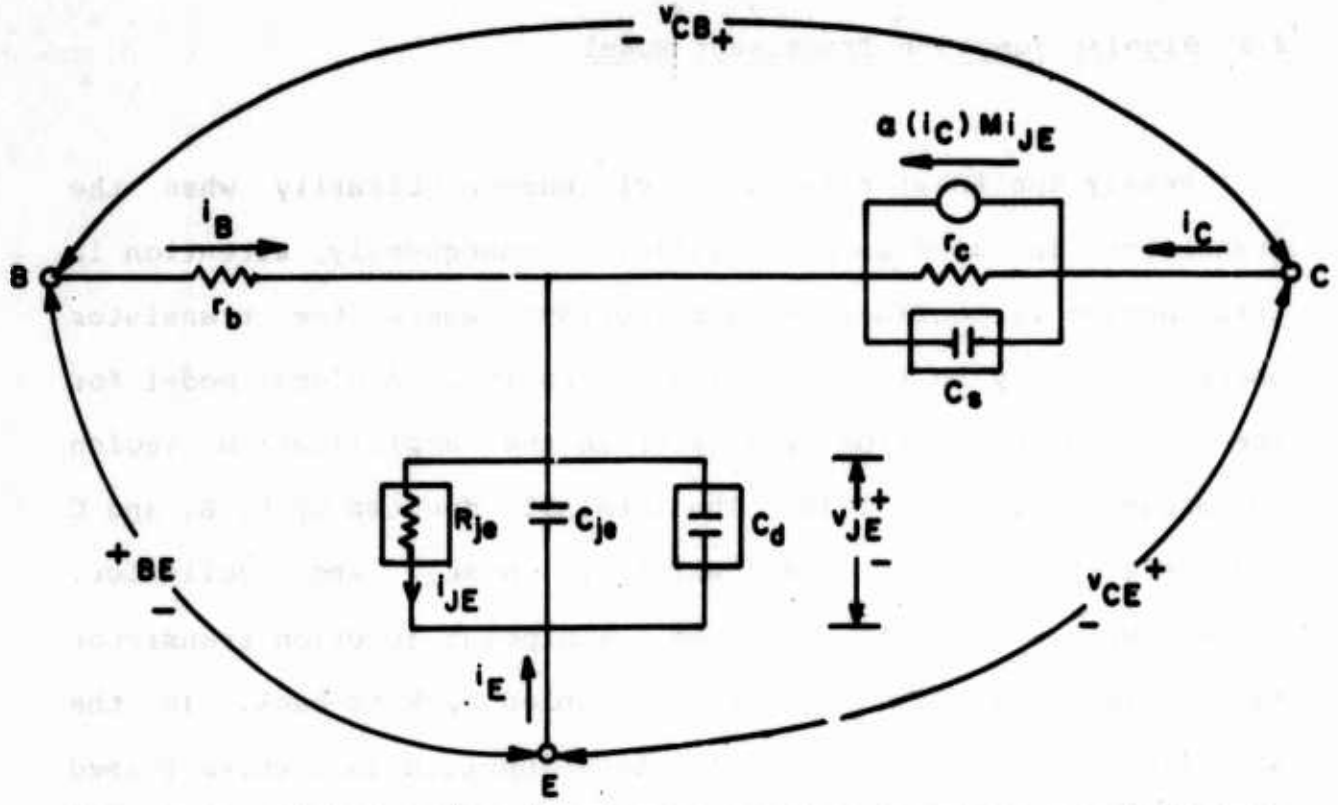

Fig. 2.10 Global model for the npn bipolar junction transistor in the amplification region.

3) C_{je}, the base-emitter junction diffusion capacitance.

4) C_d, the nonlinear emitter-base junction diffusion capacitance whose value depends linearly on the emitter-base junction current in accordance with

$$C_d = C_2' \, i_{JE} \quad . \tag{2.6-2}$$

5) $\alpha(i_c)Mi_{JE}$, the collector current-controlled current source. Note that the control variable i_{JE} is the emitter-base junction diode current.

6) r_c, the collector-base junction leakage resistance.

7) C_s, the nonlinear collector-base junction space charge capacitance which is given by

$$C_s = K V_{CB}^{-\mu} \quad , \quad V_{CB} > 0 \tag{2.6-3}$$

The parameters which appear in the controlled source and in (2.6-1), (2.6-2), and (2.6-3) are defined as follows:

I_s = reverse saturation current of the emitter-base diode,

q = electron charge = 1.6×10^{-19} coulombs,

k = Boltzmann's constant = 1.38×10^{-23} joules/degree Kelvin,

T = junction absolute temperature in degrees Kelvin,

n = emitter-base diode nonideality factor,

C_2' = emitter-base junction diffusion capacitance constant,

$\alpha(I_C)$ = common-base normal-mode dc current gain = $-I_C/I_E$.

The dependence on collector current is given by

$$\alpha(i_C) = \frac{h_{FE_{max}}}{1 + h_{FE_{max}} + a \log_{10}^2 \left(\frac{I_C}{I_{C_{max}}} \right)} \tag{2.6-4}$$

where $h_{FE_{max}}$ is the maximum dc current gain I_C/I_B, $I_{C_{max}}$ is the collector current at which I_C/I_B is a maximum, and a is a constant,

M = the avalanche multiplication factor given by

$$M = \left[1 - \left(\frac{V_{CB}}{V_{CB0}} \right)^{\eta} \right]^{-1} \tag{2.6-5}$$

where V_{CBO} is the avalanche voltage and n is the avalanche exponent,

K = collector-base junction space charge capacitance at 1 volt collector-base voltage,

μ = collector-base junction grading constant.

To obtain the nonlinear incremental equivalent circuit for the bipolar junction transistor, it is necessary to expand in power series the incremental currents through the nonlinear elements R_{je}, C_d, C_s, and $\alpha(i_C)Mi_{JE}$. Since NCAP is based upon nodal analysis, all of these expansions must be in terms of incremental voltages.

The incremental current through R_{je} may be written as

$$i_{je}(t) = \sum_{k=1}^{\infty} g_k [v_{je}(t)]^k \qquad (2.6\text{-}6)$$

where the linear incremental emitter resistance of the transistor is defined to be

$$r_e = \frac{1}{g_1} = \frac{nkT}{q(-I_E)} \qquad (2.6\text{-}7)$$

and

$$g_k = \frac{1}{k(-I_E)} \; g_1 \; g_{k-1} \qquad (2.6\text{-}8)$$

The series expansion for the incremental current through C_d is

$$i_{cd}(t) = \sum_{k=0}^{\infty} \frac{C_{dk}}{k+1} \frac{d}{dt} \{ [v_{je}(t)]^{k+1} \} \qquad (2.6\text{-}9)$$

where

$$C_{d0} = C_2' (-I_E) \qquad (2.6\text{-}10)$$

and

$$C_{dk} = C_2' g_k . \qquad (2.6\text{-}11)$$

The incremental current through C_s is

$$i_{cs}(t) = \sum_{k=0}^{\infty} \frac{C_{sk}}{k+1} \frac{d}{dt} \{ [v_{cb}(t)]^{k+1} \} \qquad (2.6\text{-}12)$$

where

$$C_{s0} = K V_{CB}^{-\mu} \qquad (2.6\text{-}13)$$

and

$$C_{sk} = \frac{(k + \mu - 1)}{kV_{CB}} C_{s(k-1)} . \qquad (2.6\text{-}14)$$

The final series to be presented is that for the

current-controlled current source $\alpha(i_C)Mi_{JE}$. This is obtained by expressing the currents i_C and i_{JE} in terms of the voltages v_{CB} and v_{JE}. It follows that the incremental current through the controlled source may be written as

$$i_s(t) = \sum_{k=1}^{\infty} q_k [v_{cb}(t), v_{je}(t)] \qquad (2.6\text{-}15)$$

where the first three terms are given by

$$\begin{aligned}
q_1(v_{cb},v_{je}) &= \alpha_1 I_{JE} m_1 v_{cb} + \alpha_1 m_0 g_1 v_{je} \\
q_2(v_{cb},v_{je}) &= (\alpha_1 I_{JE} m_2 + \alpha_2 I_{JE}^2 m_1^2) v_{cb}^2 \\
&\quad + (\alpha_1 m_1 g_1 + 2 I_{JE} m_0 m_1 g_1) v_{cb} v_{je} \\
&\quad + (\alpha_1 m_0 g_2 + \alpha_2 m_0^2 g_1^2) v_{je}^2 \\
q_3(v_{cb},v_{je}) &= (\alpha_1 I_{JE} m_3 + 2\alpha_2 I_{JE}^2 m_1 m_2 + \alpha_3 I_{JE}^3 m_1^3) v_{cb}^3 \\
&\quad + (\alpha_1 m_2 g_1 + 2\alpha_2 I_{JE} m_0 m_2 g_1 + 2\alpha_2 I_{JE} m_1^2 g_1) v_{cb}^2 v_{je} \\
&\quad + (\alpha_1 m_1 g_2 + 2\alpha_2 I_{JE} m_0 m_1 g_2 + 2\alpha_2 m_0 m_1 g_1^2) v_{cb} v_{je}^2 \\
&\quad + (\alpha_1 m_0 g_3 + 2\alpha_2 m_0^2 g_1 g_2 + \alpha_3 m_0^3 g_1^3) v_{je}^3 .
\end{aligned} \qquad (2.6\text{-}16)$$

In (2.6-16) the coefficients α_1, α_2, and α_3 are associated with

the $\alpha(i_C)$ nonlinearity of (2.6-4). They are given by

$$\alpha_1 = \frac{h_{FE_{max}}}{1 + h_{FE_{max}} + a \log_{10}^2 \left(\frac{I_C}{I_{C_{max}}} \right) + 2a \log_{10} \left(\frac{I_C}{I_{C_{max}}} \right) \log_{10} e}$$

$$\alpha_2 = -\alpha_1^3 \frac{a \log_{10} e}{3h_{FE_{max}} I_C^2} \left[\log_{10} \left(\frac{I_C}{I_{C_{max}}} \right) + \log_{10} e \right] , \qquad (2.6\text{-}17)$$

$$\alpha_3 = \frac{2\alpha_2^2}{\alpha_1} - \frac{\alpha_1 \alpha_2}{3I_C} - \frac{\alpha_1^4 a \log_{10}^2 e}{3h_{FE_{max}} I_C^2}$$

Also, in (2.6-16), the coefficients m_0, m_1, m_2, and m_3 are generated from the avalanche nonlinearity of (2.6-5). They are

$$m_0 = \left[1 - \left(\frac{V_{CB}}{V_{CBO}} \right)^{\eta} \right]^{-1} ,$$

$$m_1 = \frac{\eta}{V_{CBO}^{\eta}} m_0^2 V_{CB}^{\eta-1} ,$$

$$m_2 = \frac{m_1^2}{m_0} + \frac{(\eta-1)m_1}{2V_{CB}} , \qquad (2.6\text{-}18)$$

$$m_3 = \frac{2}{3} m_2 \left[\frac{2m_1}{m_0} + \frac{\eta-1}{2V_{CB}} \right] - \frac{m_1}{3} \left[\frac{m_1^2}{m_0^2} + \frac{\eta-1}{2V_{CB}^2} \right] .$$

When the transistor is biased well outside of the avalanche region (i.e., $V_{CB} << V_{CBO}$), m_0 is approximately unity while m_1, m_2,

and m_3 are extremely small. The terms in (2.6-16) involving v_{CB} can then be ignored.

The nonlinear incremental equivalent circuit for the npn bipolar junction transistor is shown in Fig. 2.11. This model is suitable for nodal analysis because the voltages v_{je} and v_{cb} are readily expressed in terms of node-to-datum voltages.

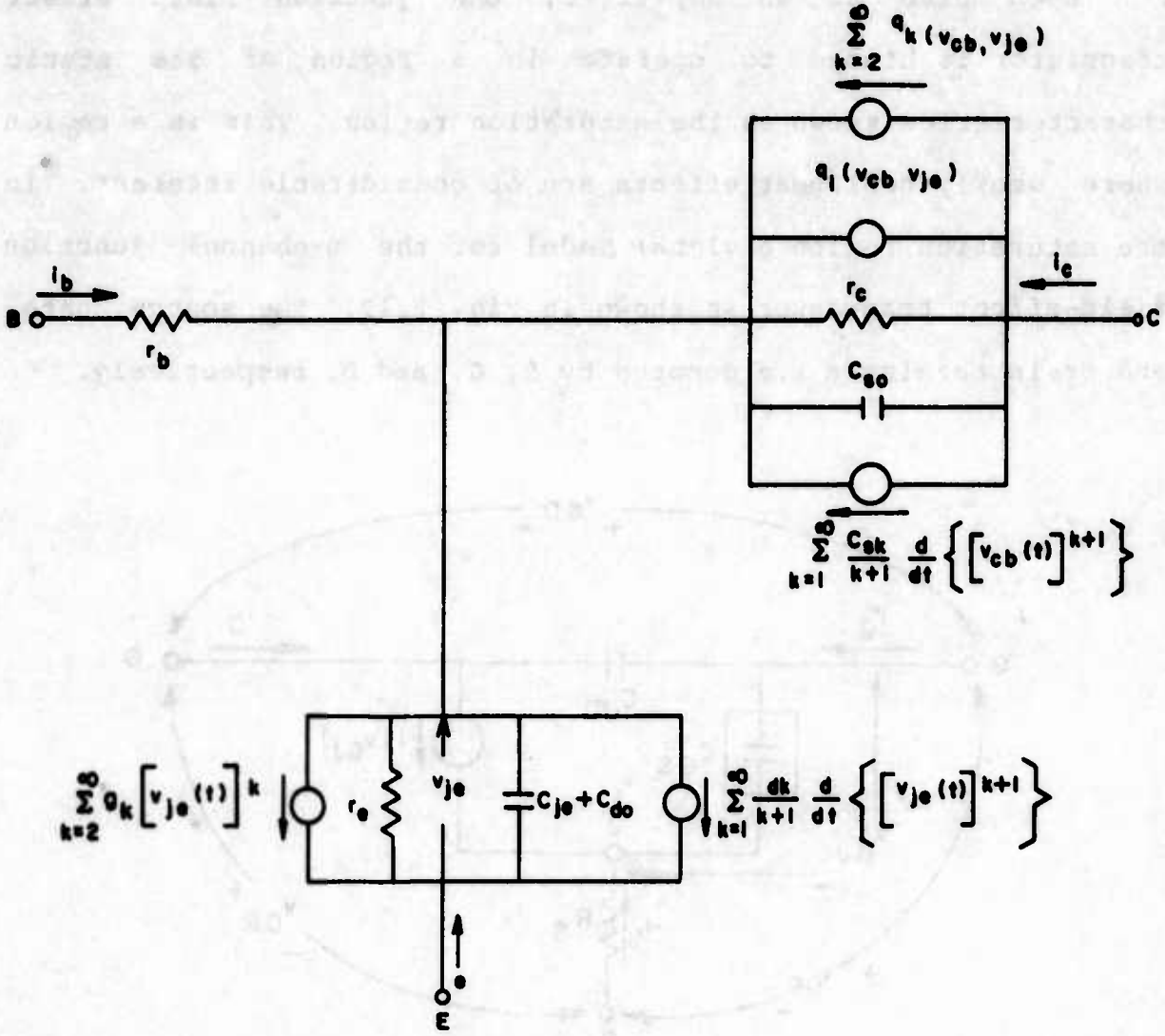

Fig. 2.11 Nonlinear incremental equivalent circuit for npn bipolar junction transistor in the amplification region.

2.7 Junction Field-Effect Transistor Model

When used as an amplifier, the junction field effect transistor is biased to operate in a region of its static characteristics known as the saturation region. This is a region where weakly nonlinear effects are of considerable interest. In the saturation region a global model for the n-channel junction field-effect transistor is shown in Fig. 2.12. The source, gate, and drain terminals are denoted by S, G, and D, respectively.

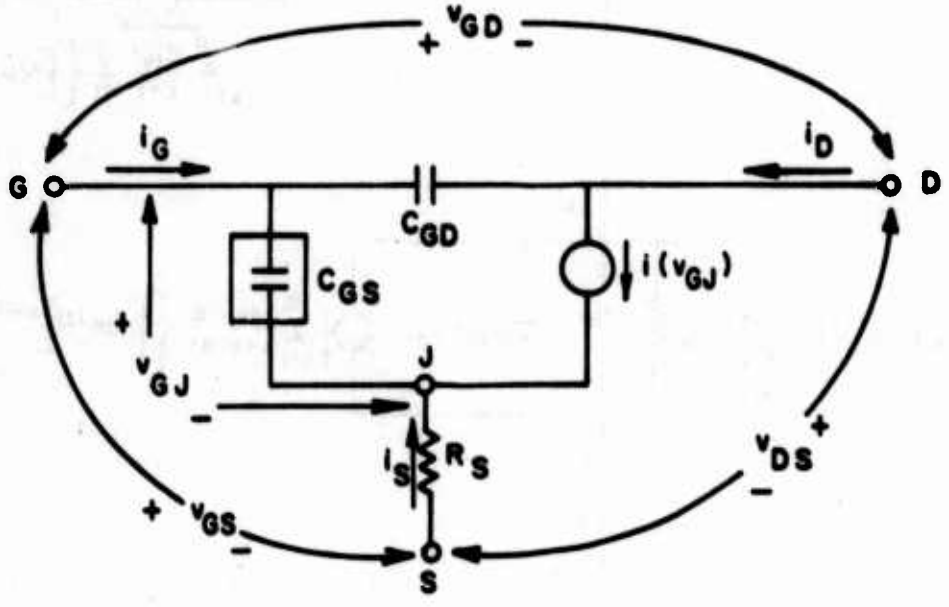

Fig. 2.12 Global model for the n-channel junction field-effect transistor in the saturation region.

The p-channel junction field-effect transistor has the same global model except that all voltages and current are of opposite polarity.

The four elements in the global model are

1) R_S, the source bulk resistance.

2) $i(v_{GJ})$, a nonlinear voltage-controlled current source. Note that the control variable v_{GJ} is the voltage between the gate terminal and the internal node denoted by J. In the saturation region an analytical expression for $i(v_{GJ})$ is

$$i(v_{GJ}) = 3I_{D_{max}} \frac{1-e^{-\Gamma}}{2\Gamma^2} \left\{ -\frac{1-e^{-\Gamma}}{\Gamma^2} + \sqrt{\left(\frac{1-e^{-\Gamma}}{\Gamma^2}\right)^2 + 4\left(\frac{1}{3} - \frac{v_{GJ}+\psi}{V_p+\psi}\right) + \frac{2}{3}\left(\frac{v_{GJ}+\psi}{V_p+\psi}\right)^{\frac{3}{2}}} \right\} \tag{2.7-1}$$

3) C_{GS}, the nonlinear gate-to-source capacitance which is given by

$$K\,(-V_o - V_{GJ})^{-m} \quad , \quad v_{GJ} < 0 \quad . \tag{2.7-2}$$

4) C_{GD}, the gate-to-drain capacitance.

The parameters which appear in (2.7-1) and (2.7-2) are defined as follows:

$I_{D_{max}}$ = drain current at maximum dc current gain,

V_p = pinchoff voltage,

ψ = JFET barrier potential,

Γ = JFET parameter given by

$$\Gamma = \frac{V_p}{E_c L_g} \qquad (2.7\text{-}3)$$

Where E_c is a critical field value associated with the mobility and L_g is the gate length,

V_o = gate-to-source capacitance built-in voltage,

K = gate-to-source capacitance for $-V_o - v_{GJ} = 1$,

m = gate-to-source capacitance exponent.

The incremental current through the nonlinear controlled source $i(v_{GJ})$ may be expressed as

$$i(v_{gj}) = \sum_{k=1}^{\infty} g_k \left[v_{gj}(t) \right]^k \qquad (2.7\text{-}4)$$

To simplify the expressions for the coefficients, let

$$\rho = \frac{1-e^{-\Gamma}}{\Gamma^2}$$

$$B = \frac{V_{GJ} + \psi}{V_p + \psi} \qquad (2.7\text{-}5)$$

$$A = \rho^2 + 4\left[\frac{1}{3} - B + \frac{2}{3} B^{\frac{3}{2}}\right]$$

The first three coefficients are then given by

$$g_1 = \frac{3I_{D_{max}}}{V_p + \psi}^{\rho} \quad \frac{-1 + B^{\frac{1}{2}}}{A^{\frac{1}{2}}}$$

$$g_2 = \frac{3I_{D_{max}}}{4(V_p+\psi)^2}^{\rho} \quad \frac{AB^{-\frac{1}{2}} - 4[-1 + B^{\frac{1}{2}}]^2}{A^{\frac{3}{2}}} \qquad (2.7\text{-}6)$$

$$g_3 = \frac{I_{D_{max}}}{8(V_p+\psi)^3}^{\rho} \quad \frac{-A^2B^{-\frac{3}{2}} - 12AB^{-\frac{1}{2}}[-1 + B^{\frac{1}{2}}] + 48[-1 + B^{\frac{1}{2}}]^3}{A^{\frac{5}{2}}}$$

The series expansion for the incremental current through the gate-to-source capacitance is

$$i_{cgs}(t) = \sum_{k=0}^{\infty} \frac{C_{gsk}}{k+1} \frac{d}{dt} \{ v_{gj}(t)^{k+1} \} \qquad (2.7\text{-}7)$$

where

$$C_{gs0} = K(-V_o - V_{GJ})^{-m} \qquad (2.7\text{-}8)$$

and

$$C_{gsk} = k\frac{(k + m - 1)}{(-V_o - V_{GJ})} C_{gs(k-1)} \qquad (2.7\text{-}9)$$

The nonlinear incremental equivalent circuit for the n-channel

junction field-effect transistor is shown in Fig. 2.13.

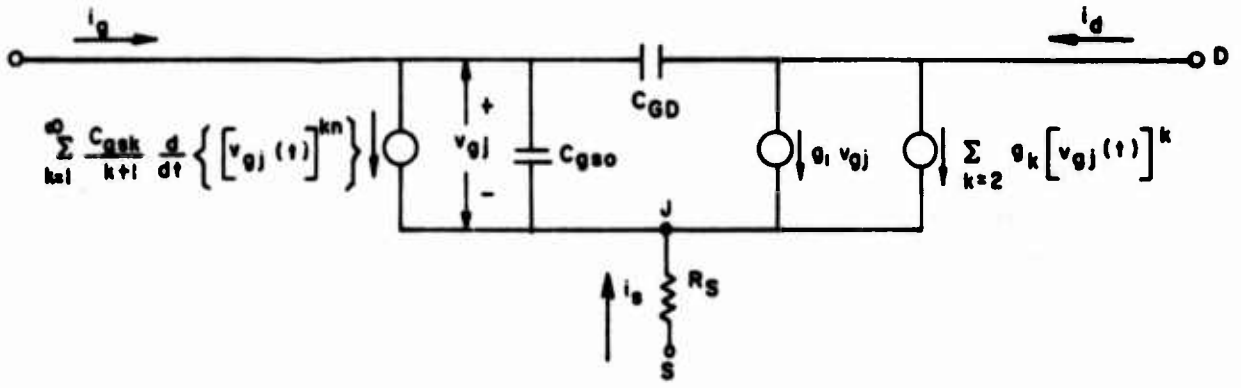

Fig. 2.13 Nonlinear incremental equivalent circuit for the n-channel junction field-effect transistor in the saturation region.

2.8 Vacuum-Tube Diode Model

The simplest vacuum tube is the vacuum-tube diode which consists of two electrodes enclosed in a vacuum. A global model for the vacuum-tube diode is presented in Fig. 2.14. The plate

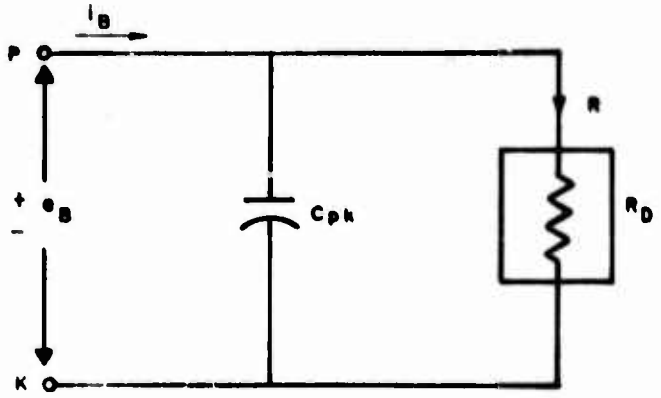

Fig. 2.14 Global model for vacuum-tube diode, $e_B > 0$.

and cathode electrodes are denoted by P and K, respectively. The two elements in the global model are

1) R_D, the nonlinear plate-to-cathode resistance. Its current-voltage relationship is given by

$$i_R = G e_B^{\frac{3}{2}} \quad , \quad e_B > 0 \quad . \tag{2.8-1}$$

2) C_{pk}, The plate-to-cathode capacitance.

The parameter which appears in (2.8-1) is defined to be

G = perveance.

The incremental current through the nonlinear resistor can be written as

$$i_r(t) = \sum_{k=1}^{\infty} g_k \left[e_b(t) \right]^k \qquad (2.8\text{-}2)$$

where the linear incremental resistance of the diode is

$$r_d = \frac{1}{g_1} = \left(\frac{3}{2} G E_B^{\frac{1}{2}} \right)^{-1} \qquad (2.8\text{-}3)$$

and

$$g_k = \frac{1}{k} \left[\frac{3}{2} - (k - 1) \right] E_B^{-1} g_{k-1} \qquad (2.8\text{-}4)$$

The nonlinear incremental equivalent circuit for the vacuum-tube diode is presented in Fig. 2.15. Note that the linear incremental

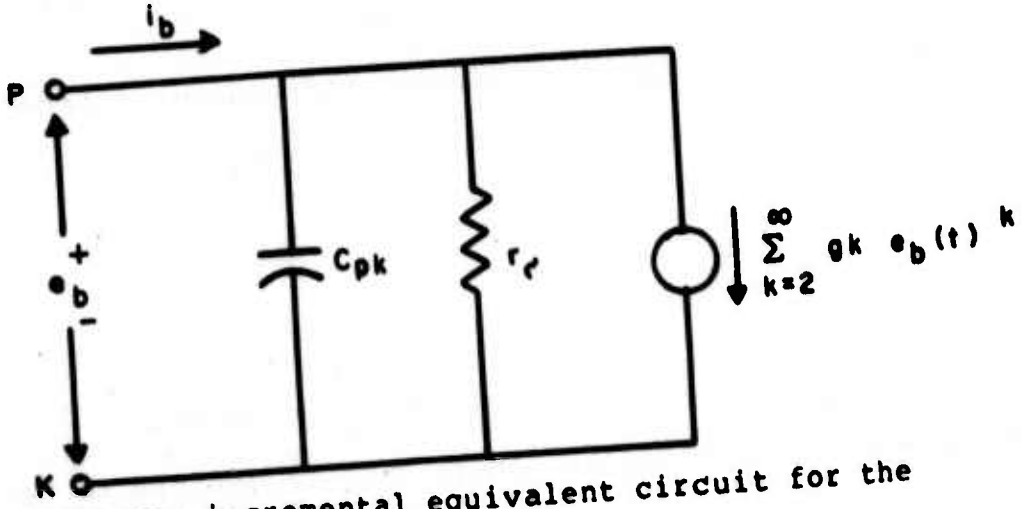

Fig. 2.15 Nonlinear incremental equivalent circuit for the vacuum-tube diode, $e_B > 0$.

circuit consists simply of the capacitor C_{pk} in parallel with the resistor r_d.

2.9 Vacuum-Tube Triode Model

Assume the vacuum-tube triode is biased to operate in its amplification region. A global model suitable for the amplification region is shown in Fig. 2.16. The grid, plate, and cathode

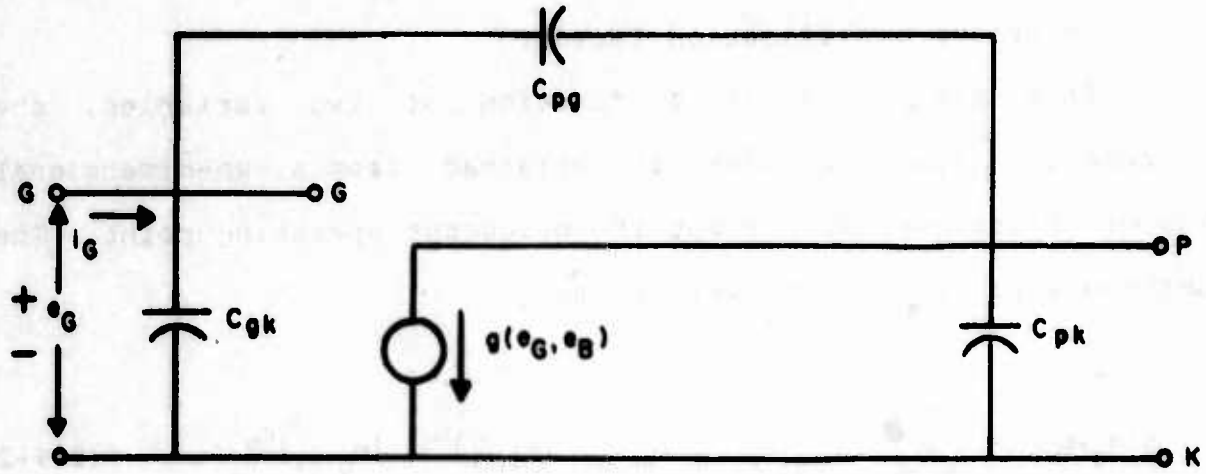

Fig. 2.16 Global model for vacuum-tube triode in the amplification region.

electrodes are denoted by G, P, and K, respectively.

The four circuit elements in the global model are:

1) C_{gk}, the grid-to-cathode capacitance.
2) C_{pg}, the plate-to-grid capacitance.
3) C_{pk}, the plate-to-cathode capacitance.
4) $g(e_G, e_B)$, the voltage-controlled current source representing the triode space current which is given by

$$g(e_G,e_B) = G_0 \left[1 - \frac{e_G}{E_{C_{max}}}\right] \left(e_G + \phi + \frac{e_B}{\mu}\right)^{\frac{3}{2}} \qquad (2.9\text{-}1)$$

The parameters which appear in (2.9-1) are defined as follows:

G_o = perveance for $e_G=0$,

$E_{C_{max}}$ = grid-to-cathode voltage for perveance equal to zero,

ϕ = offset voltage due to space charge effects,

μ = triode amplification factor.

Since $g(e_G,e_B)$ is a function of two variables, the incremental space current is obtained from a two-dimensional Taylor series expansion about the quiescent operating point. The desired expansion may be written as

$$g(e_g,e_b) = \sum_{m_1=0}^{\infty} \sum_{m_2=0}^{\infty} K_{m_1,m_2} [e_{g(t)}]^{m_1} [e_{b(t)}]^{m_2} \qquad (2.9\text{-}2)$$

$$(m_1 = m_2 \neq 0)$$

The expression for the coefficients is simplified by defining

$$G(e_G) = G_0 \left[1 - \frac{e_G}{E_{C_{max}}}\right]$$

$$f(e_G,e_B) = \left(e_G + \phi + \frac{e_B}{\mu}\right)^{\frac{3}{2}} \qquad (2.9\text{-}3)$$

It follows that

$$K_{m_1,m_2} = \frac{1}{(m_1!)\,(m_2!)} \sum_{\substack{q_1=0 \\ (q_1+q_2=m_1)}}^{1} \sum_{q_2=0}^{m_1} \frac{(q_1+q_2)!}{(q_1!)\,(q_2!)} \frac{\partial^{q_1} g(e_G)}{\partial e_G^{q_1}} \frac{\partial^{q_2+m_2} f(e_G,e_B)}{\partial e_G^{q_2}\,\partial e_B^{m_2}} \Bigg|_{\substack{e_G = E_G, \\ e_B = E_B}} . \tag{2.9-4}$$

In (2.9-4) the constraint, $q_1+q_2=m_1$, indicates that only terms for which the indices sum to m_1 are included in the double summation. The first several coefficients are given by

$$K_{0,1} = \frac{3Go}{2\mu}\left[1 - \frac{E_G}{E_{C_{max}}}\right]\left[E_G + \phi + \frac{E_B}{\mu}\right]^{\frac{1}{2}}$$

$$K_{1,0} = \frac{3Go}{2}\left[1 - \frac{E_G}{E_{C_{max}}}\right]\left[E_G + \phi + \frac{E_B}{\mu}\right]^{\frac{1}{2}} - \frac{Go}{E_{C_{max}}}\left[E_G + \phi + \frac{E_B}{\mu}\right]^{\frac{3}{2}}$$

$$K_{0,2} = \frac{3Go}{8\mu^2}\left[1 - \frac{E_G}{E_{C_{max}}}\right]\left[E_G + \phi + \frac{E_B}{\mu}\right]^{-\frac{1}{2}}$$

$$K_{1,1} = \frac{3Go}{4\mu}\left[1 - \frac{E_G}{E_{C_{max}}}\right]\left[E_G + \phi + \frac{E_B}{\mu}\right]^{-\frac{1}{2}} - \frac{3Go}{2\mu E_{C_{max}}}\left[E_G + \phi + \frac{E_B}{\mu}\right]^{\frac{1}{2}}$$

$$K_{2,0} = \frac{3Go}{8}\left[1 - \frac{E_G}{E_{C_{max}}}\right]\left[E_G + \phi + \frac{E_B}{\mu}\right]^{-\frac{1}{2}} - \frac{3Go}{2E_{C_{max}}}\left[E_G + \phi + \frac{E_B}{\mu}\right]^{\frac{1}{2}} \tag{2.9-5}$$

The degree of a term in (2.9-2) is the sum of its exponents. Hence, $K_{m1,m2}$ is the coefficient of a term having degree $(m1+m2)$. It is convenient to denote by $g_k(e_g,e_b)$ the sum of all terms in (2.9-2) having degree k. Then (2.9-2) may be expressed as

$$g(e_g,e_b) = \sum_{k=1}^{\infty} g_k\ (e_g,e_b) \qquad (2.9\text{-}6)$$

where the first three terms are given by

$$g_1(e_g,e_b) = K_{0,1}\, e_b + K_{1,0}\, e_g \equiv \frac{1}{r_p}\, e_b + g_m\, e_g$$

$$g_2(e_g,e_b) = K_{0,2}\, e_b^2 + K_{1,1}\, e_g\, e_b + k_{2,0}\, e_g^2$$

$$g_3(e_g,e_b) = K_{0,3}\, e_b^3 + K_{1,2}\, e_g\, e_b^2 + k_{2,1}\, e_g^2\, e_b + k_{3,0}\, e_g^3$$

(2.9-7)

The nonlinear incremental equivalent circuit for the vacuum-tube triode is shown in Fig. 2.17. Note that $K_{0,1} \equiv \frac{1}{r_p}$ is the reciprocal

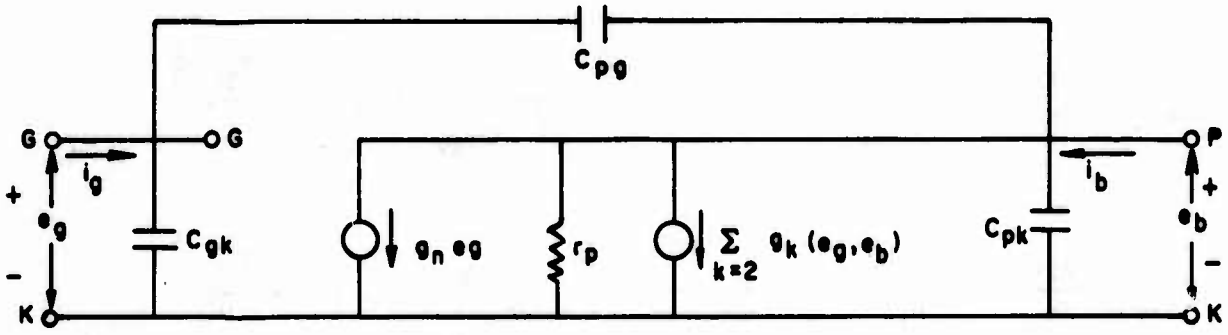

Fig. 2.17 Nonlinear incremental equivalent circuit for the vacuum-tube triode in the amplification region.

of the triode plate resistance while $K_{1,0} \equiv g_m$ is the triode

transconductance or mutual conductance.

2.10 Vacuum-Tube Pentode Model

For the vacuum-tube pentode, attention is also focused on the amplification region. A global model suitable for this region is shown in Fig. 2.18. The control grid, screen grid, suppressor grid, plate, and cathode terminals are denoted by G_1,

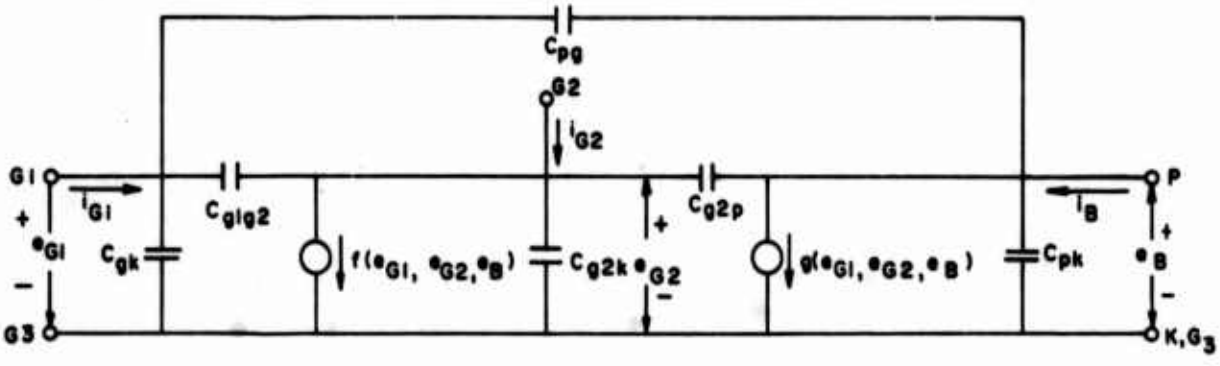

Fig. 2.18 Global model for vacuum-tube pentode in the amplification region.

G_2, G_3, P, and K, respectively. Since the suppressor terminal G_3 s typically tied to the cathode K, the two electrodes are shown as a single terminal in the figure. The interelectrode capacitances are represented by C_{gk}, $C_{g_1g_2}$, C_{g_2k}, C_{g_2p}, C_{pk}, and C_{pg}. The remaining two circuit elements in the global model are:

1) $f(e_{G1}, e_{G2}, e_B)$, the voltage-controlled current source representing the space current between the cathode and screen which is given by

$$f(e_{G_1},e_{G_2},e_B) = G_0 \left[1 - \frac{e_{G_1}}{E_{C_{max}}}\right] \left(e_{G_1} + \phi + \frac{e_{G_2}}{\mu}\right)^{\frac{3}{2}} \frac{\frac{1}{D}}{\frac{1}{D} + \left(\frac{e_B}{e_{G_2}}\right)^m}$$

(2.10-1)

2) $g(e_{G1}, e_{G2}, e_B)$, the voltage-controlled current source representing the space current between the cathode and plate which is given by

$$g(e_{G_1},e_{G_2},e_B) = G_0 \left[1 - \frac{e_{G_1}}{E_{C_{max}}}\right] \left(e_{G_1} + \phi + \frac{e_{G_2}}{\mu}\right)^{\frac{3}{2}} \frac{\left(\frac{e_B}{e_{G_2}}\right)^m}{\frac{1}{D} + \left(\frac{e_B}{e_{G_2}}\right)^m}$$

(2.10-2)

The parameters which appear in (2.10-1) and (2.10-2) are defined as follows:

G_o = perveance for $e_{G1}=0$,

E_{cmax} = control grid-to-cathode voltage for perveance equal to zero,

ϕ = offset voltage due to space charge effects,

μ = control grid amplification factor,

D = space current division constant,

m = space current division exponent.

A nonlinear incremental equivalent circuit for the pentode, which is appropriate in the amplification region, is obtained by

expanding $f(e_{G1}, e_{G2}, e_B)$ and $g(e_{G1}, e_{G2}, e_B)$ in three-dimensional Taylor series about the quiescent operating point. In particular,

$$f(e_{g1},e_{g2},e_b) = \sum_{n1=0}^{\infty}\sum_{n2=0}^{\infty}\sum_{n3=0}^{\infty} A_{n1,n2,n3}\, e_{g1}^{n1}\, e_{g2}^{n2}\, e_b^{n3} \qquad (2.10\text{-}3)$$

$$n1=n2=n3 \neq 0$$

and

$$g(e_{g1},e_{g2},e_b) = \sum_{n1=0}^{\infty}\sum_{n2=0}^{\infty}\sum_{n3=0}^{\infty} B_{n1,n2,n3}\, e_{g1}^{n1}\, e_{g2}^{n2}\, e_b^{n3} \qquad (2.10\text{-}4)$$

$$n1=n2=n3 \neq 0$$

where the coefficients $A_{n1, n2, n3}$ and $B_{n1, n2, n3}$ are given by

$$A_{n1,n2,n3} = \frac{1}{(n1!)(n2!)(n3!)} \left.\frac{\partial^{(n1+n2+n3)} f(e_{G1},e_{G2},e_B)}{\partial e_{G1}^{n1}\, \partial e_{G2}^{n2}\, \partial e_B^{n3}}\right|_{\substack{e_{G1}=E_{G1}\\ e_{G2}=E_{G2}\\ e_B=E_B}} \qquad (2.10\text{-}5)$$

and

$$B_{n1,n2,n3} = \frac{1}{(n1!)(n2!)(n3!)} \left.\frac{\partial^{(n1+n2+n3)} g(e_{G1},e_{G2},e_B)}{\partial e_{G1}^{n1}\, \partial e_{G2}^{n2}\, \partial e_B^{n3}}\right|_{\substack{e_{G1}=E_{G1}\\ e_{G2}=E_{G2}\\ e_B=E_B}} \qquad (2.10\text{-}6)$$

Because of the complexity of (2.10-5) and (2.10-6), explicit expressions for the coefficients are not used by NCAP for their

evaluation. Instead the partial derivatives are carried out numerically. Recall that $A_{n1,\ n2,\ n3}$ and $B_{n1,\ n2\ ,\ n3}$ are coefficients of terms having degree (n1 + n2 + n3). It is convenient to denote by $f_k(e_{g1},\ e_{g2},\ e_b)$ and $g_k(e_{g1}\ ,\ e_{g2}\ ,\ e_b)$ the sum of all terms in (2.10-3) and (2.10-4), respectively, having degree k. Then (2.10-3) and (2.10-4) may be expressed as

$$f(e_{g1},e_{g2},e_b) = \sum_{k=1}^{\infty} f_k(e_{g1},e_{g2},e_b) \qquad (2.10\text{-}7)$$

and

$$g(e_{g1},e_{g2},e_b) = \sum_{k=1}^{\infty} g_k(e_{g1},e_{g2},e_b) \qquad (2.10\text{-}8)$$

The nonlinear incremental equivalent circuit for the vacuum-tube pentode is shown in Fig. 2.19.

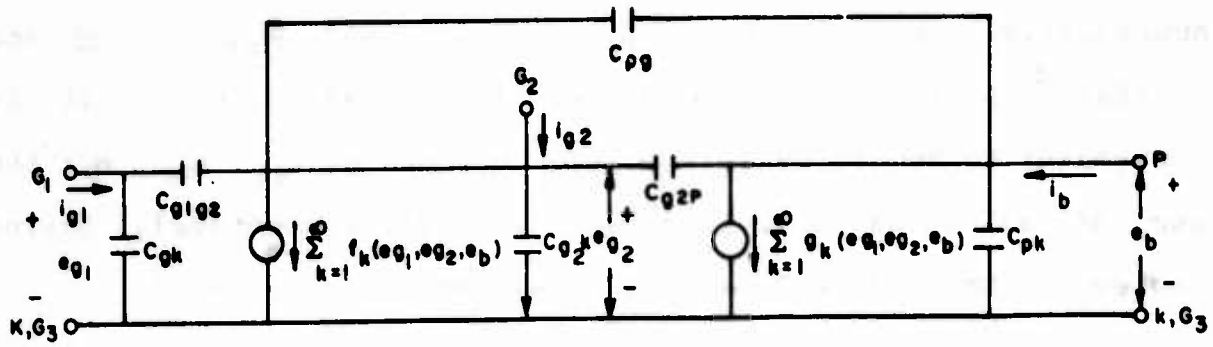

Fig. 2.19 Nonlinear incremental equivalent circuit for the vacuum-tube pentode in the amplification region.

Typically, the screen grid G_2 is connected externally to the cathode through an impedance which behaves as a short circuit at the signal frequencies of interest. As a result, e_{G2} remains approximately fixed at the dc value E_{G2} and the incremental voltage e_{g2} is approximately zero. Under this assumption, the generator $f(e_{G1}, e_{G2}, e_B)$ is incrementally shorted out and need not be considered in the incremental equivalent circuit. In addition, the generator $g(e_{G1}, e_{G2}, e_B)$ becomes

$$g(e_{G_1}, e_B) = G_0 \left[1 - \frac{e_{G_1}}{E_{C_{max}}}\right] \left(e_{G_1} + \phi + \frac{E_{G_2}}{\mu}\right)^{\frac{3}{2}} \frac{\left(\frac{e_B}{E_{G_2}}\right)^m}{\frac{1}{D} + \left(\frac{e_B}{E_{G_2}}\right)^m} \tag{2.10-9}$$

The incremental current corresponding to (2.10-9) is represented by the two-dimensional Taylor series

$$g(e_{g_1}, e_b) = \sum_{n_1=0}^{\infty} \sum_{n_2=0}^{\infty} K_{n_1,n_2} e_{g_1}^{n_1} e_b^{n_2} = \sum_{k=1}^{\infty} g_k(e_{g_1}, e_b)$$

$$(n_1 = n_2 \neq 0)$$

(2.10-10)

where $g_k(e_{g1}, e_b)$ denotes the sum of all terms in (2.10-9) having degree k and the coefficients $K_{n1, n2}$ are given by

$$K_{n_1,n_2} = \frac{1}{(n_1!)(n_2!)} \left. \frac{\partial^{(n_1+n_2)} g(e_{G_1}, e_B)}{\partial e_{G_1}^{n_1} \partial e_B^{n_2}} \right|_{\substack{e_{G_1} = E_{G_1} \\ e_B = E_B}}$$

(2.10-11)

Recognizing that 1) C_{g_2k} is shorted out, 2) C_{gk} is in parallel with $C_{g_1g_2}$, and 3) C_{g_2p} is in parallel with C_{pk}, the nonlinear incremental equivalent circuit for the vacuum-tube pentode becomes that shown in Fig. 2.20. From Fig. 2.20 it is apparent that

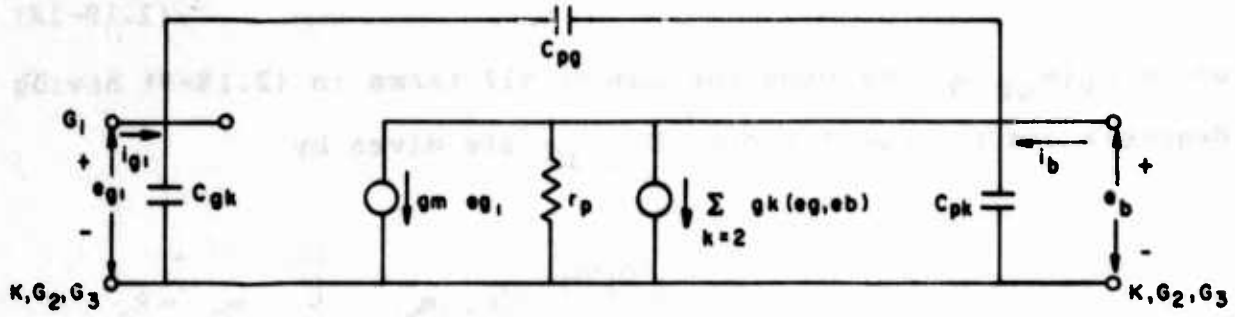

Fig. 2.20 Nonlinear incremental equivalent circuit for the vacuum-tube pentode in the amplification region under the assumption that the screen grid is incrementally shorted to the cathode.

$K_{0,1}$ and $K_{1,0}$ in (2.2.10-10) have been defined such that

$$g_1(e_{g_1}, e_b) = K_{0,1}\, e_b + K_{1,0}\, e_{g_1} \equiv \frac{1}{r_p}\, e_b + g_m\, e_{g_1} \quad . \quad (2.10\text{-}12)$$

Hence, the simplified pentode model of Fig. 2.20 is identical in form to the triode model of Fig. 2.17.

SECTION 3

NONLINEAR MODEL PARAMETERS FOR SEMICONDUCTOR DEVICES AND VACUUM TUBES

SECTION 3: NONLINEAR MODEL PARAMETERS FOR SEMICONDUCTOR DEVICES AND VACUUM TUBES

3.1 Introduction

In order to use NCAP to calculate nonlinear transfer functions and subsequently determine the interference to electronic circuits, a detailed circuit model must be constructed. Part of this model construction includes using the stored models for semiconductor devices and vacuum tubes within the computer code which take into account their inherent nonlinear behavior. In so doing, the parameters relevant to a given device model must be determined. This section will illustrate how the device parameters can be obtained so that a detailed circuit model can be constructed.

In this section, nonlinear model parameters for a semiconductor diode, a bipolar junction transistor (BJT), a junction field effect transistor (JFET), and vacuum tube diode, triode and pentode will be determined. The techniques employed in determining these parameters are recommended techniques, i.e. they are not the sole means for determining the required parameters. However, the techniques reported upon in this section have been used with a sufficient degree of confidence, success and accuracy.[1,2,3,4]

There are three basic techniques for obtaining parameter values for the models used in NCAP. The first is an engineering guess of the nominal parameter values. This could yield

inaccurate results and will not be discussed in this section. The second technique employs manufacturers data sheets. The use of data sheet information will be cited where applicable. A major drawback with this technique is, in general, insufficient data are provided to determine all of the model parameters. The third technique is the measurement technique. This will be the major topic of discussion in this section. A combination of dc, pulse and high frequency measurements will be addressed relevant to the parameter values for the various models.

It is appropriate to mention at this point that there are two factors relevant to parameter value determination and, therefore, circuit model construction, which are not explicitly accounted for in the stored NCAP device models. These are 1) parasitic effects, such as bond wire, lead inductances, and fringing capacitances, and 2) thermal effects. Parasitic components can be added externally to the device models. Thermal effects can be partially accounted for by modifying appropriate parameter values to reflect actual temperature at the operating point.

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2. J. F. Spina, J. Lexa, D. D. Weiner, "Computer Modeling of a Solid-State VHF Tuner Using the Nonlinear Transfer Function Approach," Technical Memorandum, Rome Air Development Center, Griffiss Air Force Base, New York, 1974.
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4. J. J. Whalen, C. A. Paludi, Jr. and T. F. Fang, "Applications of the Nonlinear Circuit Analysis Program NCAP," 1977 IEEE International Electromagnetic Compatability Symposium Record, pp. 467-474, Seattle, Washington, August 1977. (IEEE Pub. No. 770H 1231-0 EMC)

3.2 Nonlinear Model Parameters for the Semiconductor Diode

Figure 3.2-1 illustrates the model for the semiconductor diode used by NCAP.[1] Additional information about how NCAP calculates the nonlinear transfer functions using this model is addressed in detail in Section 2.5.

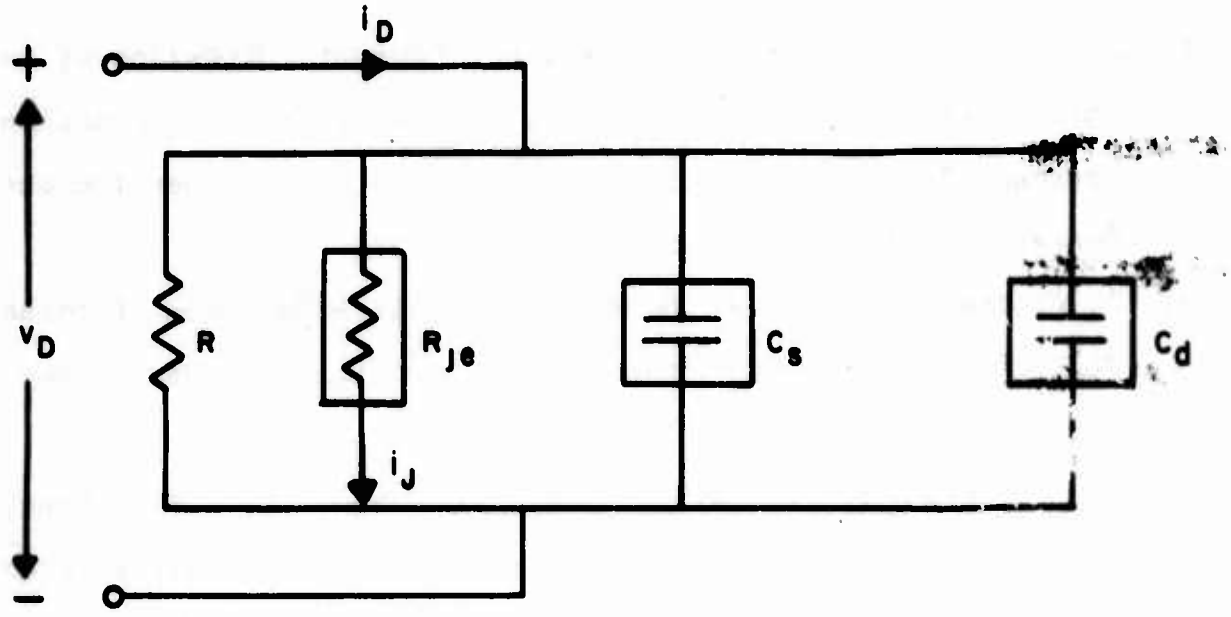

Fig. 3.2-1 Global model for semiconductor diode

This model actually represents two different models; one for the diode in the forward bias region, and one for the diode in the reverse bias region.

The parameters required by NCAP to use this model are given in Table 3.2-1. Determination of these parameters will be addressed in subsequent subsections.

TABLE 3.2-1

NCAP SEMICONDUCTOR DIODE MODEL PARAMETERS

NO.	NAME	UNITS	DESCRIPTION
1[a]	I_D	A	dc bias current diode
2[a]	n		diode non-ideality factor
3[a]	C_j	F	forward biased junction capacitance extrapolated to zero current
4[a]	C_j'	F	derivative of junction capacitance with respect to current
1[b]	V_D	V	magnitude of dc reverse bias voltage
2[b]	K	F	varactor capacitance at 1 volt reverse bias
3[b]	μ	--	varactor capacitance exponent
4[b]	R	Ω	reverse bias leakage resistance

a--forward bias
b--reverse bias

3.2.1 Forward Biased Semiconductor Diode

A typical forward biased diode is illustrated in Fig. 3.2-2

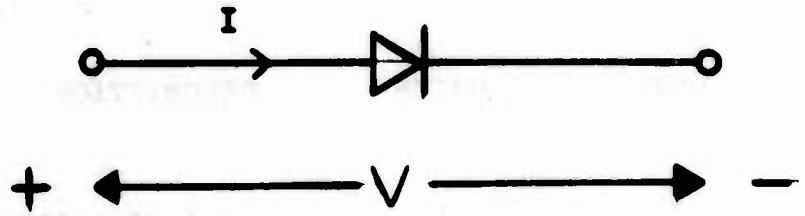

Fig. 3.2-2 Forward biased diode

The portion of the global model given in Fig. 3.2-1, used by NCAP in the forward biased region, is given in Fig. 3.2-3.

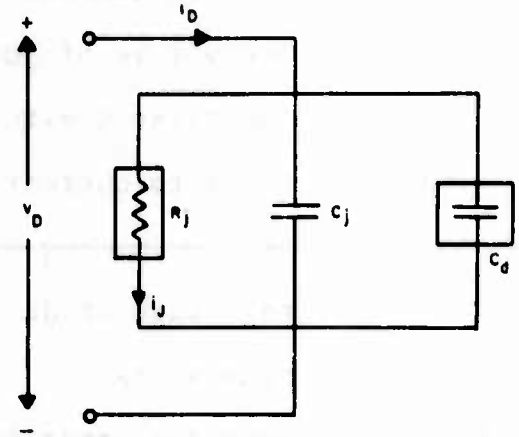

Fig. 3.2-3 Global model for semiconductor diode in forward biased region

The NCAP parameter I_D, dc bias current, is simply the dc current at the operating point (Q pt.).

The diode nonideality factor, n, is obtained by measuring the dc forward current-voltage characteristic which is governed by the mathematical relationship given in Eq. 3.2-1.

$$i_J = I_s \left[\exp \left(\frac{qv_D}{nkT} \right) - 1 \right] \qquad (3.2\text{-}1)$$

In the forward bias region, the -1 term can be neglected. Based upon Eq. 3.2-1, a semi-log plot of I_F vs V_F can be made. I_F is the dc forward bias current plotted on the ordinate (log scale) and V_F is the dc forward biased voltage plotted on the abscissa (linear scale). A typical I-V plot is illustrated in Fig. 3.2-4.

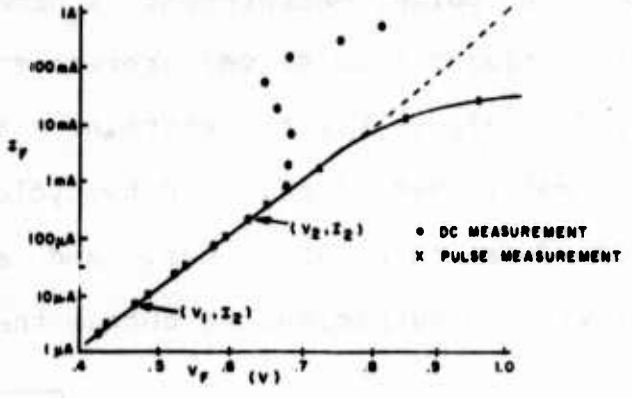

Fig. 3.2-4 Typical I-V plot for determining n

The simplest means of determining the data required for the plot I_F vs V_F is a dc measurement shown in Fig. 3.2-5.

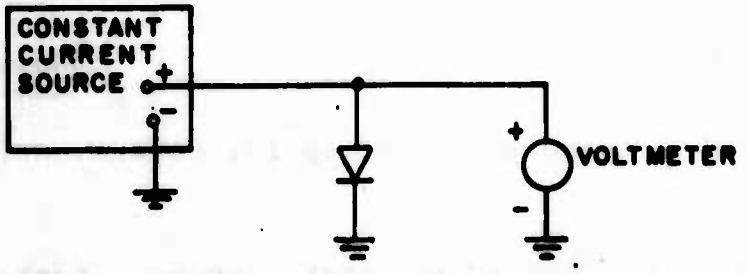

Fig. 3.2-5 dc measurement set up for determination of n

A transistor curve tracer can also be used to make dc

measurements to obtain the appropriate data (see Section 3.3.1).

Since the diode model used in NCAP does not explicitly account for thermal effects, measurement techniques for determining parameter values should be chosen such that undesirable thermal effects are minimized. When dc measurements are used to determine n, erroneous data may result at current levels greater than 10 mA. This is illustrated in Fig. 3.2-4. To overcome these effects, a pulse measurement scheme may be used.[2] Figure 3.2-6 illustrates a pulse measurement scheme used to obtain the necessary data (I_F vs V_F) to determine n at higher current levels, i.e. greater than 10 mA. A duty cycle of 10 to 50 mS (or a typical pulse duration of 300 sec, and a typical PRF of 100 pulses/sec) will be sufficient to obtain the required data.

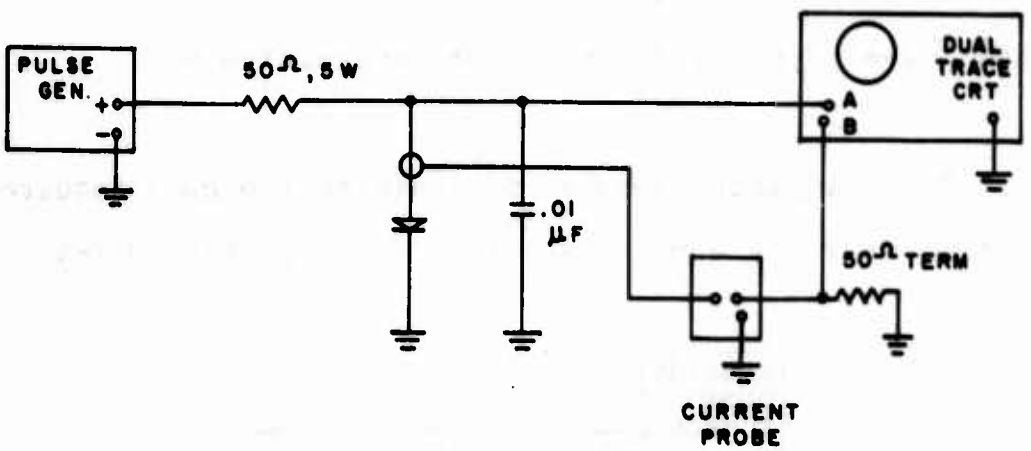

Fig. 3.2-6 Pulse measurement set up for determination of n

It should be mentioned that under normal (typical) conditions, a value of n can be assumed to be equal to 1.0.

The diode nonideality factor, n, can be calculated using the data plotted in Fig. 3.2-4 and Eq. 3.2-2.

$$n = (q/kT) (V_{F2} - V_{F1}) / \ln (I_{F2}/I_{F1}) \qquad (3.2\text{-}2)$$

The capacitive effects in the forward biased region are due to the nonlinear diffusion capacitance of the p-n junction, C_d. The relationship governing this effect is given by Eq. 3.2-3.

$$C_d = C_j' \, i_{JE} \qquad (3.2\text{-}3)$$

NCAP requires two parameters to characterize this phenomena: C_j, the forward biased junction capacitance extrapolated to zero current, and C_j', the derivative of junction capacitance with respect to current. A capacitance bridge can be used to obtain the necessary data to construct a linear plot of C vs I_F. Figure 3.2-7 shows the diode connection on a Boonton Capacitance Bridge.

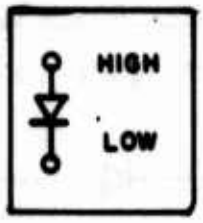

Fig. 3.2-7 Diode connection on capacitance bridge

A plot of C vs I_F (on linear scales) is shown in Fig. 3.2-8.

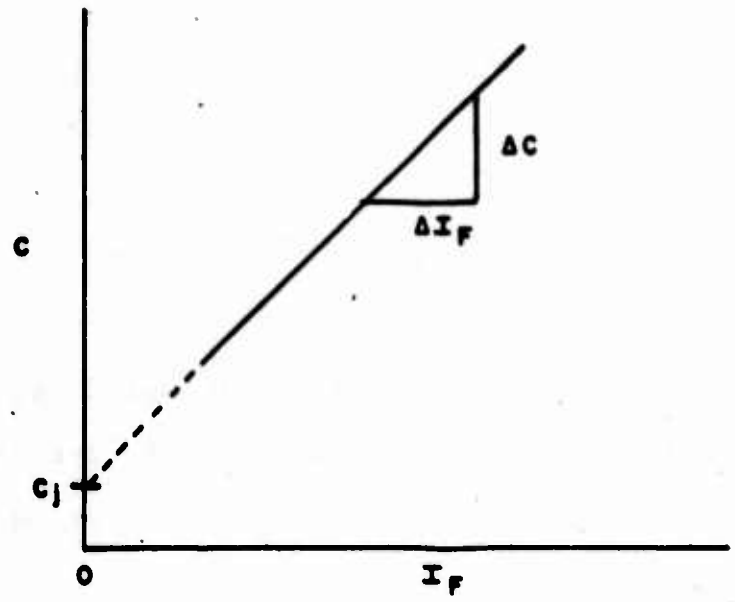

Fig. 3.2-8 Typical plot of C vs I

The value for C_j can be obtained by inspection by extrapolating the data to $I_F = 0$. C_j' is the slope of the straight line data.

$$C_j' = \Delta C / \Delta I_F \qquad (3.2\text{-}4)$$

3.2.2 Reverse Biased Semiconductor Diode

A typical reverse biased diode is illustrated in Fig. 3.2-9.

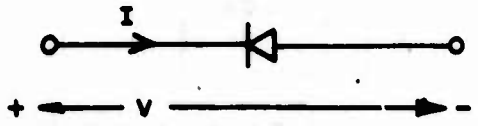

Fig. 3.2-9 Reverse biased diode

The portion of the global model given in Fig. 3.2-1, used by NCAP in the reverse biased region, is given in Fig. 3.2-10.

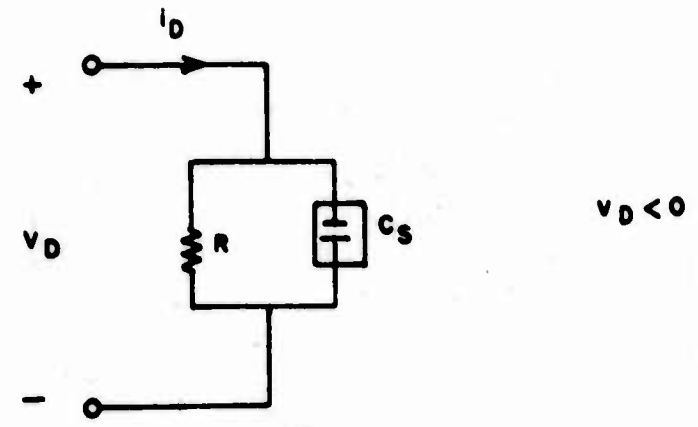

Fig. 3.2-10 Global model for semiconductor diode in reverse biased region.

The NCAP parameter V_D, magnitude of the dc reverse bias voltage, is simply the dc voltage at the reverse bias operating point.

The reverse bias leakage resistance, R, is obtained from the dc measurement scheme illustrated in Fig. 3.2-11.

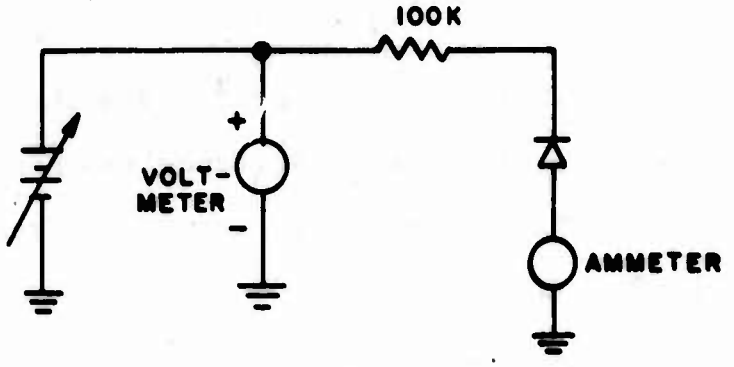

Fig. 3.2-11 Experimental set-up for determining reverse biased dc leakage resistance R

A characteristic plot (on linear coordinates) can be made from the measured data. A typical plot of reverse current (I_R) in nA vs reverse voltage (V_R) in V is shown in Fig. 3.2-12.

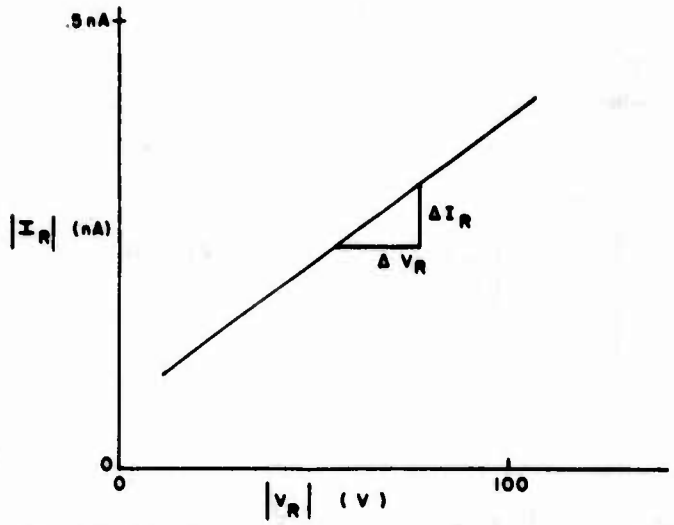

Fig. 3.2-12 Typical plot of I_R vs V_R for determining diode leakage resistance, R

The value for R can be determined by:

$$R = \frac{\Delta V_R}{\Delta I_R} \qquad (3.2\text{-}5)$$

The NCAP parameters K, varactor capacitance at 1 volt reverse bias and μ, varactor capacitance exponent, characterize the nonlinear transition capacitance in the reverse bias region as indicated by Eq. (3.2-6).

$$C_s = K\,(-v_D)^{-\mu} \qquad v_D < 0 \qquad (3.2\text{-}6)$$

A log-log plot of capacitance, C, vs reverse voltage (magnitude), V_R, can be obtained by using capacitance bridge measurement techniques (see Fig. 3.2-13).

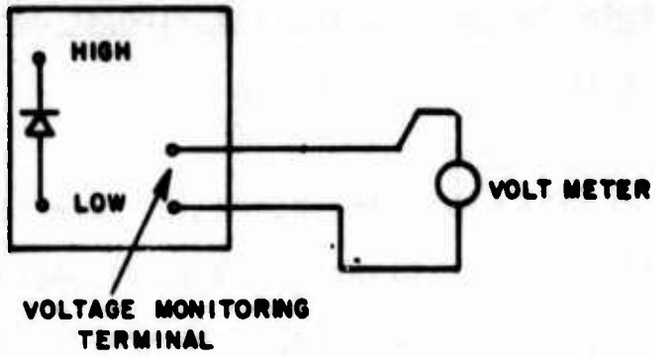

Fig. 3.2-13 Measurement set up for determining reverse biased diode parameters K and μ

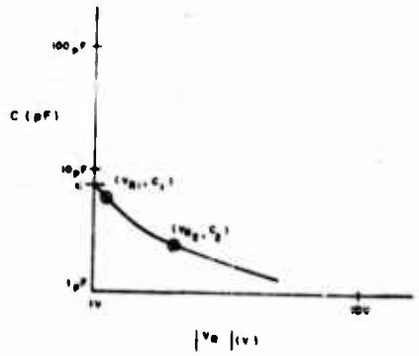

Fig. 3.2-14 Typical plot of C vs V_R

The curve of C vs V_D will result in a straight line when plotted on log-log coordinates. Using Eq. 3.2-6:

$$\log_{10} C_s = \log_{10} K - \mu \log_{10} | V_D | \qquad (3.2\text{-}7)$$

where $|V_R|$ from Fig. 3.2-14 equals $| V_R |$. The value K can be determined by inspection of Fig. 3.2-14. The value μ is the slope of the C vs V_R curve.

3.3 Nonlinear Model Parameters for the Bipolar Junction Transistor (BJT)

The model for the BJT in NCAP is referred to as the nonlinear T model.[1,5,6] Figure 3.3-1 illustrates the linear incremental T model. From this model, the nonlinear behavior of the BJT is accounted for as shown in Section 2.

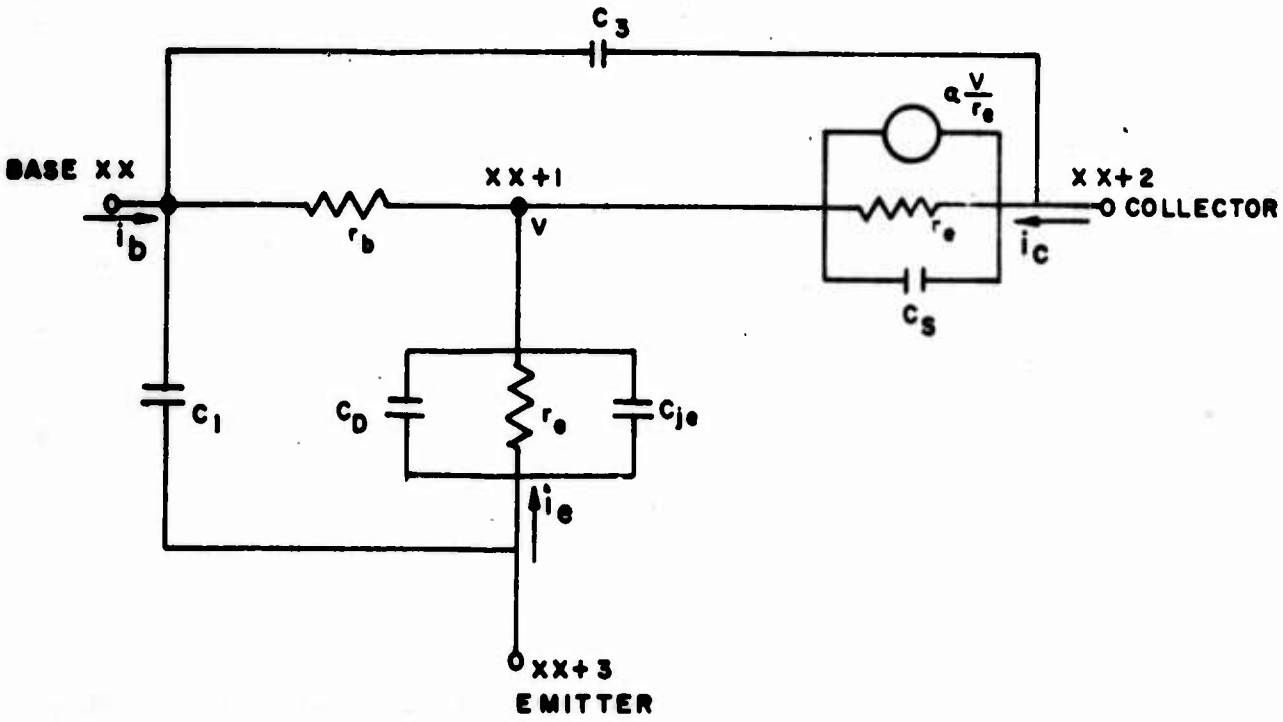

Fig. 3.3-1 Linear incremental T model for BJT

TABLE 3.3-1 lists the parameters required by NCAP to characterize the BJT. Also given are the order of input and the units of each parameter.

TABLE 3.3-1

NCAP BJT Model Parameters

Number	Name	Description	Units
1	η	Avalanche exponent	
2	V_{CB}	Collector-base bias voltage	V
3	V_{CBO}	Avalanche voltage	V
4	μ	Collector capacitance exponent	
5	I_C	Collector bias current	A
6	$I_{C_{max}}$	Collector current at maximum dc current gain	A
7	a	h_{FE} nonlinearity coefficient	
8	$h_{FE_{max}}$	Maximum dc current gain	
9	K	Collector capacitor scale factor	$F \cdot V^{\frac{1}{2}}$
10	n	Diode nonideality factor	
11	C_{je}	Base-emitter junction space charge capacitance	F
12	C_2'	Derivative of base-emitter diffusion capacitance	F/A
13	r_b	Base resistance	Ω
14	r_c	Collector resistance	Ω
15	C_1	Base-emitter capacitance	F
16	C_3	Base-collector and overlap capacitance	F

It should be mentioned that certain measured data have signs that depend upon whether the transistor is npn or pnp. Table 3.3-2 indicates the parameters of concern, their signs when measured under normal conditions in the amplification region, and the sign convention used by NCAP. Note that NCAP requires positive values for these parameters independent of the type of transistor.

TABLE 3.3-2

Sign Conventions for NCAP BJT Parameters

Parameter	Sign(npn)	Sign(pnp)	Sign NCAP
V_{CB}	+	-	+
V_{CBO}	+	-	+
I_C	+	-	+
$I_{C_{max}}$	+	-	+

3.3.1 n - Diode Nonideality Factor and r_b - Base Resistance

The diode nonideality factor (n) will be considered first. The value for r_b can be determined from data required by n. Several techniques for determining n will be illustrated. These techniques will result in a characteristic plot based on the current/voltage relationship given in Eq. (3.3-1) for the base-emitter junction biased under normal conditions in the

amplification region, i.e. the emitter-base junction is forward biased and the collector-base junction is reverse biased.

$$-I_E = I_{ES} \left[\exp \left(\frac{qV_{BE}}{nkT} \right) - 1 \right] \qquad (3.3\text{-}1)$$

Based on Eq. (3.3-1), a plot of dc emitter current ($-I_E$) on a log ordinate versus the dc base-emitter voltage (V_{BE}) on a linear abscissa can be made. A typical plot is illustrated in Fig. 3.3-2.

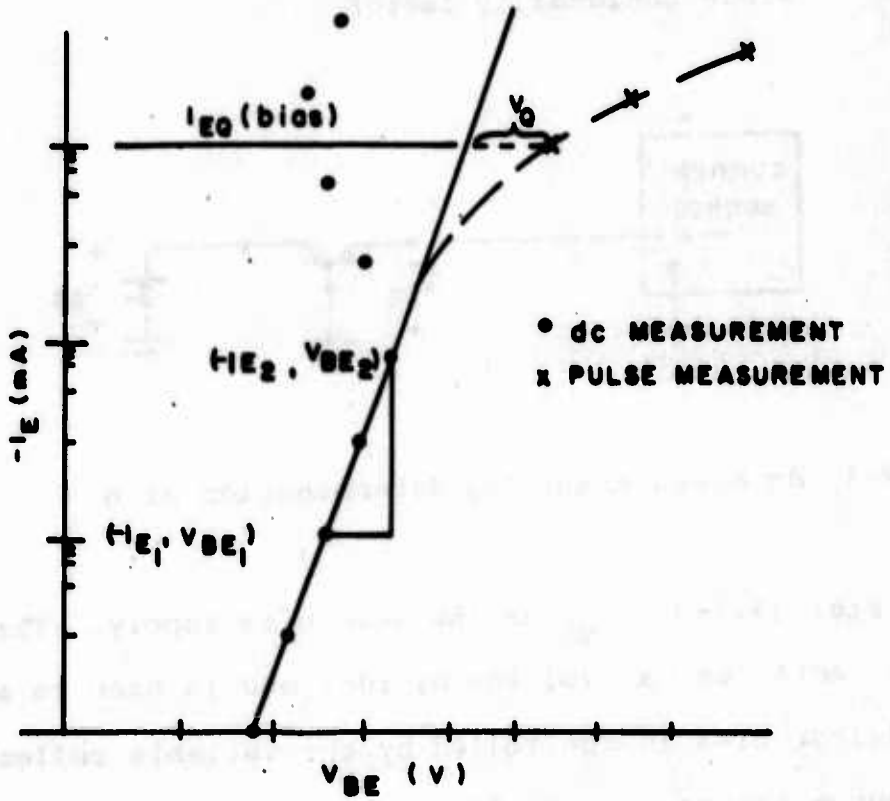

Fig. 3.3-2 Typical plot of $-I_E$ vs V_{BE}

Figures 3.3-3 and 3.3-4 illustrate dc experimental set ups for obtaining the characteristic plot of I_E vs V_{BE}.

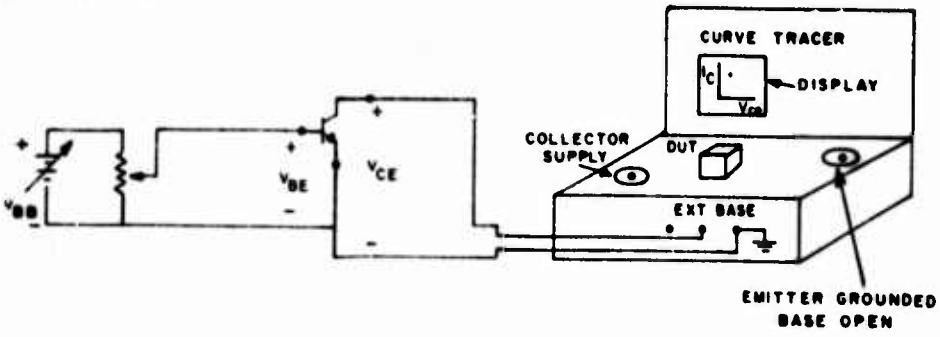

Fig. 3.3-3 Experimental setup used in determination of diode nonideality factor

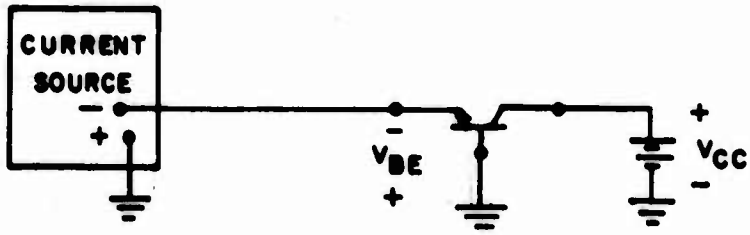

Fig. 3.3-4 dc Measurement for determination of n

In Fig. (3.3-3), V_{BB} is the base bias supply. The variable resistor acts as a voltage divider and is used to adjust V_{BE}. The collector bias is controlled by the variable collector supply on the curve tracer (internally). This may vary with V_{BE} due to a voltage drop across the internal resistance of the curve tracer. V_{CE} must be kept constant, at the operating point (Q pt.) voltage, by adjusting the collector supply. The collector current (I_C) is displayed on the curve tracer by a dot. Since

$-I_E = I_B + I_C$, and I_B is much less than I_C, then $-I_E = I_C$. Therefore, $-I_E$ vs V_{BE} can be plotted as shown in Fig. 3.3-2. Figure 3.3-4 illustrates a simplified technique for obtaining $-I_E$ and V_{BE} directly.

It is observed, using the test setups in Fig. 3.3-3 and 3.3-4, that the dc measurements of $\log(-I_E)$ vs V_{BE} deviate from a straight line because of increased junction temperatures, high level injection effects and the fact that the base-emitter junction is actually a distributed R-C network.[2,7,8] Typically, dc measurement are valid up to $-I_E = .1$ mA. For $-I_E > .1$ mA, a pulse measurement scheme is used to obtain the required data. Figure 3.3-5 shows the pulse measurement setup and the results are illustrated on Fig. 3.3-2.

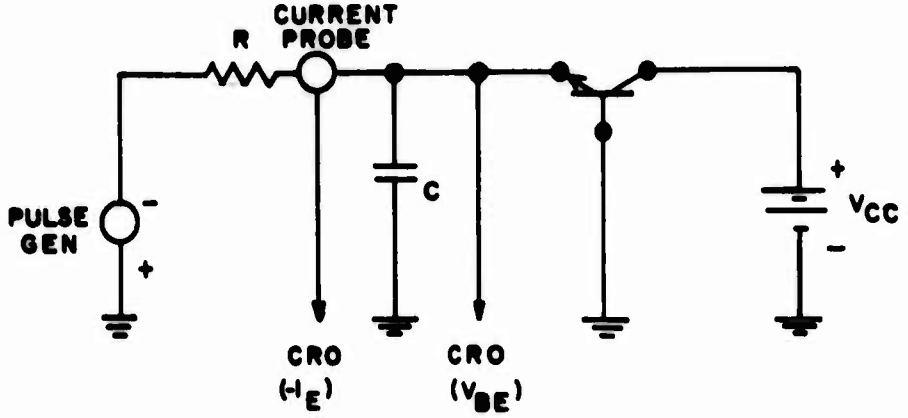

Fig. 3.3-5 Pulse measurement scheme for determination of $-I_E$ vs V_{BE}

A duty cycle of 1 to 5% is typically sufficient to obtain the necessary data.

From the results plotted in Fig. 3.3-2, n can be determined by:

$$n = (q/kT)\ (V_{BE2} - V_{BE2})\ /\ \ln\ (I_{E2}/I_{E1}) \qquad (3.3\text{-}2)$$

The base resistance is a difficult parameter to measure because the internal base node, xx + 1, shown in Fig. 3.3-1, is an inaccessible node. The simplest way to obtain r_b is to use the dc base-emitter characteristics as shown in Fig. 3.3-2. The value of r_b simply equals:

$$r_b = V_Q/I_{EQ} \qquad (3.3\text{-}3)$$

where I_{EQ} is the emitter bias current and V_Q is obtained from the plot of $-I_E$ vs V_{BE} (Fig. 3.3-2). A more precise value for r_b can be determined using high frequency measurements, i.e. s-parameters and y-parameters. Using y-parameters:

$$y_{11} = i_b/v_{in} \qquad v_{out} = 0 \qquad (3.3\text{-}4)$$

$$y_{11} \approx \frac{1}{r_b + h_{fe}\ r_e} \qquad (3.3\text{-}5)$$

Solving for r_b

$$r_b \approx \frac{1}{y_{11}} - h_{fe}(nkT/q(-I_E)) \qquad (3.3\text{-}6)$$

where h_{fe} and y_{11} can be obtained by using a network analyzer, n is the diode non-ideality factor, k = Boltzmann's Constant, T is temperature (preset at 300°K), q is the electronic charge and $-I_E$ is the dc operating point emitter current. This information can also be determined from s-parameter data.[9] Manufactures data sheets often provide Smith Chart plots of s_{11} (s_{ie}). The value of r_b can be determined from that value of the plot which is purely resistive.[10]

3.3.2 I_C - dc Collector Bias Current, $I_{C_{max}}$ - Collector Current at Maximum dc Current Gain, a - h_{FE} Nonlinearity Coefficient, $h_{FE_{max}}$ - Maximum dc Current Gain

The parameters I_C, $I_{C_{max}}$, h_{FE}, $h_{FE_{max}}$ and are related by an empirical relationship given by Eq. 3.3-7.

$$h_{FE} = \frac{h_{FE\ MAX}}{1 + a \log_{10}^2 \left(\frac{I_C}{I_{CMAX}} \right)} \qquad (3.3\text{-}7)$$

To obtain these parameters, a characteristic plot must be made of h_{FE} on the ordinate versus I_C on a log abscissa. A typical plot of h_{FE} vs I_C is illustrated in Fig. 3.3-6.

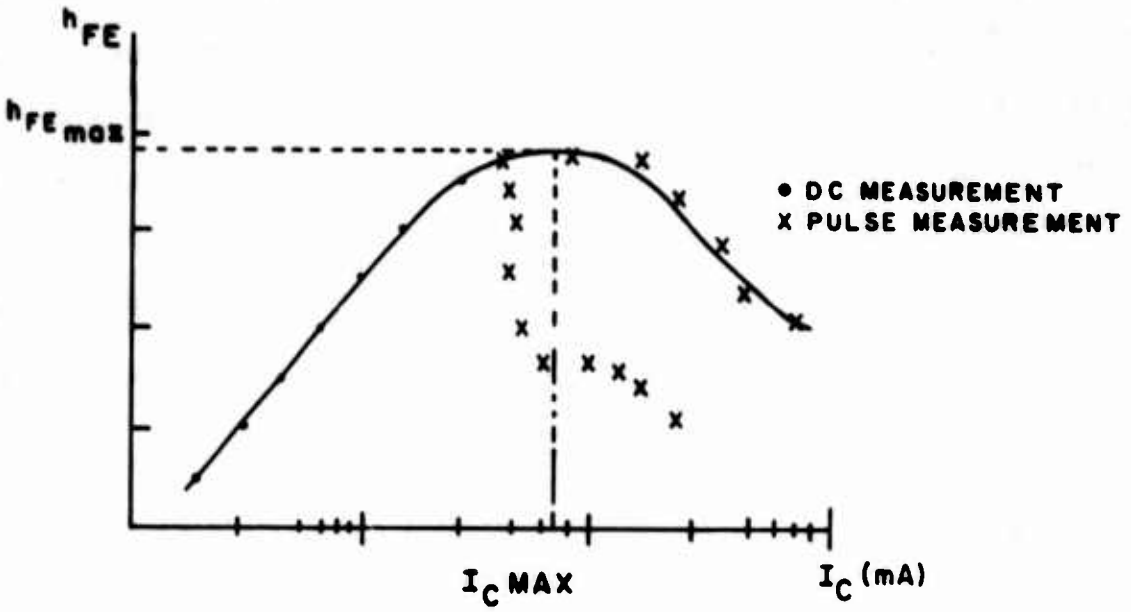

Fig. 3.3-6 Typical plot of h_{FE} vs I_C

There are three basic techniques for obtaining the necessary data to plot h_{FE} vs I_C. The first technique employs a transistor curve tracer. The common-emitter output characteristics are displayed on the curve tracer. Values for I_{B_k} and I_{C_k} can be determined by inspection (see Fig. 3.3-7). Note that I_{B_k}'s can be determined from the number of steps displayed on the curve tracer, and I_{C_k}'s are obtained by a straight line extrapolation of the I_{B_k} curve to the I_C axis.

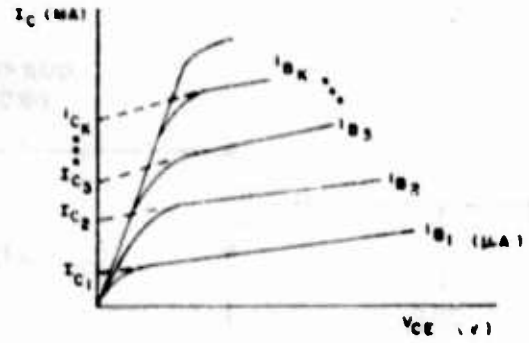

Fig. 3.3-7 Common-emitter output characteristics

Since $h_{FE} = I_{C_k}/I_{B_k}$, h_{FE} vs I_C can be plotted as shown in Fig. 3.3-6.

A more direct means for measuring the necessary dc currents is illustrated in Fig. 3.3-8.

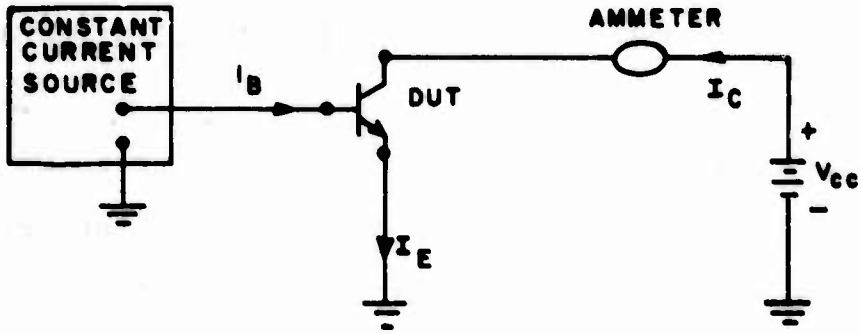

Fig. 3.3-8 Experimental setup for determination of h_{FE} nonlinear parameters

These measurement techniques are dc techniques and are valid for low current levels, i.e. $I_C < 1$ mA. For high current levels, i.e., $I_C > 1$mA, a pulse measurement technique is used. This technique is illustrated in Fig. 3.3-9.

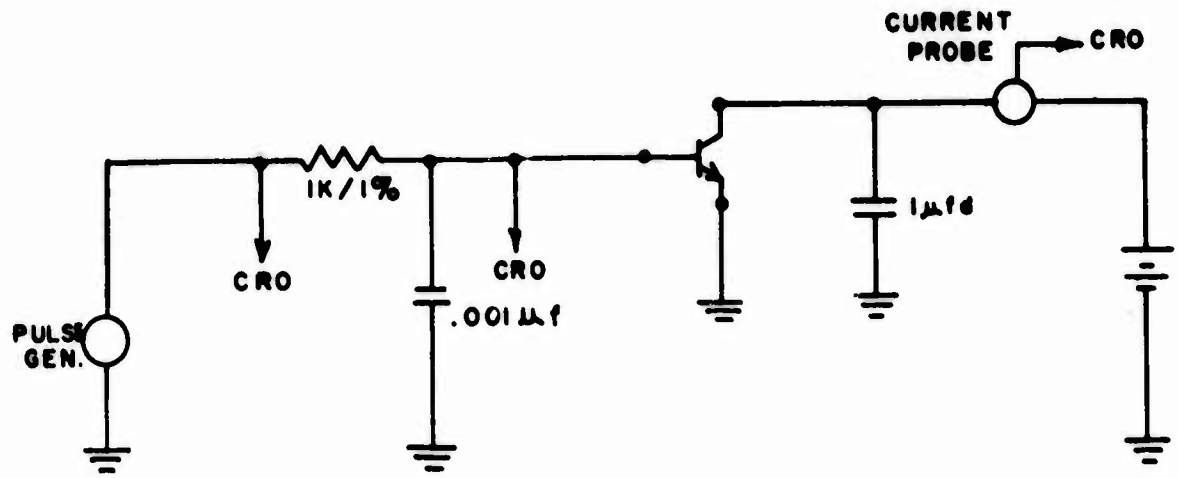

Fig. 3.3-9 Pulse measurement system for determination of h_{FE} vs I_C.

A duty cycle of 1 to 5% is typically sufficient to obtain the necessary data.

From the characteristic plot of h_{FE} vs I_C as shown in Fig. 3.3-6, $h_{FE_{max}}$, and $I_{C_{max}}$ can be determined by inspection; the value for (a) has to be calculated. The h_{FE} nonlinearity coefficient (a) can be calculated in two ways, first at the Q pt., based upon the value of I_C, or, over a given range. At the Q pt.:

$$a = \left[\left(\frac{h_{FE\ MAX}}{h_{FE}} \right) - 1 \right] / \left[\log_{10}^2 \left(\frac{I_C}{I_{CMAX}} \right) \right] \qquad (3.3\text{-}8)$$

and over a given range, say (I_{C1}, h_{FE1}) and (I_{C2}, h_{FE2}) where $I_{C1} < I_C < I_{C2}$

$$a = [h_{FE2} - h_{FE1}]/[h_{FE1} \log_{10}^2 (\frac{I_{C1}}{I_{CMAX}}) - h_{FE2} \log_{10}^2 (\frac{I_{C2}}{I_{CMAX}})]$$

(3.3-9)

3.3.3 η - Avalanche Exponent, V_{CB} - Collector-Base Bias Voltage, V_{CBO} - Avalanche Voltage, r_c - Collector Resistance

The avalanche effects in the BJT model are accounted for by an avalanche multiplication factor (M). The value for M is calculated internally by NCAP. However, values for η, V_{CB} and V_{CBO} must be provided. These parameters can be determined from the common-base characteristics of the BJT. Figure 3.3-10 illustrates the typical common-base characteristics as displayed on a transistor curve tracer.

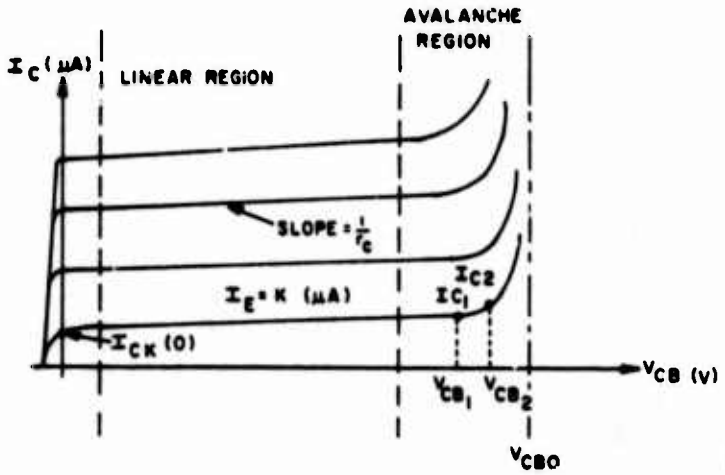

Fig. 3.3-10 Typical common-base characteristics of BJT

The value of r_c can be determined from the slope of the I_C curve corresponding to the dc emitter current I_E. Denote this slope by m. Then

$$r_c = \frac{1}{m} \qquad (3.3\text{-}10)$$

The parameter value n can be calculated using two data points (I_{C1} and I_{C2}) given in Fig. 3.3-10 and Eq. 3.3-11.

$$n = \frac{\log_{10} \left\{ \frac{B_2}{B_1} \left(\frac{B_1 - I_{CK}(0)}{B_2 - I_{CK}(0)} \right) \right\}}{\log_{10} \left(\frac{V_{CB1}}{V_{CB2}} \right)} \qquad (3.3\text{-}11)$$

where

$$B_1 = I_{C1} - \frac{V_{CB1}}{r_c}$$

$$B_2 = I_{C2} - \frac{V_{CB2}}{r_c}$$

The value for V_{CBO} can be determined two ways. It can be estimated from the I_C vs V_{CB} characteristics as shown in Fig. 3.3-10, or it can be calculated from Eq 3.3-12.

$$V_{CB0} = \frac{V_{CB}}{\left[1 - \frac{I_{Ck}(0)}{I_C - \frac{V_{CB}}{r_c}} \right]^{\frac{1}{\eta}}} \qquad (3.3\text{-}12)$$

where V_{CB} and I_C are values measured in the avalanche region.

3.3.4 μ - Collector Capacitance Exponent, K - Collector Capacitance Scale Factor

Associated with the collector-base junction is a varactor capacitor effect governed by Eq. 3.3-13.

$$C_c = K|V_{CB}|^{-\mu} \qquad (3.3\text{-}13)$$

Values for the parameters K and μ can be obtained from a log-log plot of C_c vs $|V_{CB}|$ using Eq. 3.3-13.

$$\log_{10} C_c = \log_{10} K - \mu \log_{10}|V_{CB}| \qquad (3.3\text{-}14)$$

Equation 3.3-14 results in a straight line when plotted on log-log coordinates. K is the value of capacitance where $|V_{CB}|$ = 1 volt and $-\mu$ is the slope of the line. Figure 3.3-11 shows a typical plot of C_c vs $|V_{CB}|$.

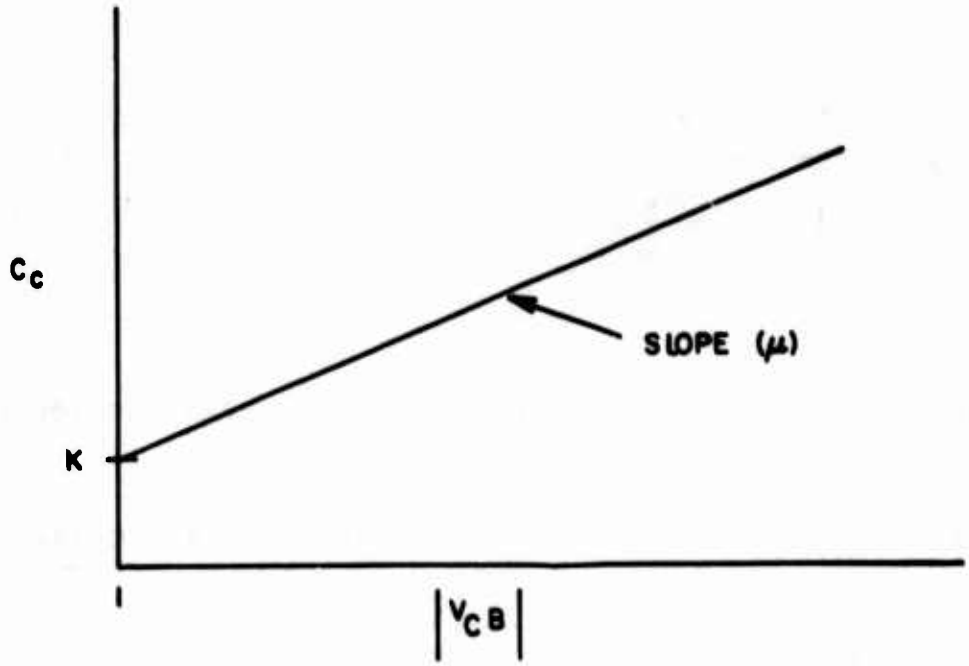

Fig. 3.3-11 Typical plot of C_c vs $|V_{CB}|$

In order to determine K and μ, C_c must be measured as a function of $|V_{CB}|$. When an RX meter is used, the collector and emitter leads are connected across the terminals of the meter, and the base and emitter leads are shorted together. The necessary data can then be obtained. When a capacitance bridge is used, Fig. 3.3-12 illustrates how the device under test should be connected to obtain the appropriate data.

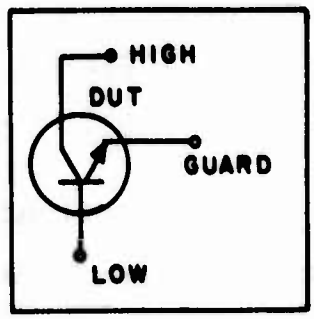

Fig. 3.3-12 Device connection pattern to determine NCAP parameters K and μ on capacitance bridge

3.3.5 C_{je} - Base-Emitter Junction Space Charge Capacitance

C_2' - Derivative of Base-Emitter Diffusion Capacitance

The parameters required to characterize the base-emitter junction capacitance effects can be obtained in a similar fashion as those for the collector-base junction. Figure 3.3-13 shows the connections using a capacitance bridge to obtain a plot of C_2 vs $-I_E$. The mathematical relationship which governs these effects is given in Eq. 3.3-15.

$$C_2 = C_{je} + C_2' i_{je} \tag{3.3-15}$$

where C_2 is the parallel combination of C_{je} and C_d. When C_2 vs $-I_E$ is plotted on linear coordinates, the plot is a straight line. Values for C_{je} and C_2' can be determined by inspection. C_{je} is the intercept and C_2' is the slope of the line (see Fig. 3.3-14).

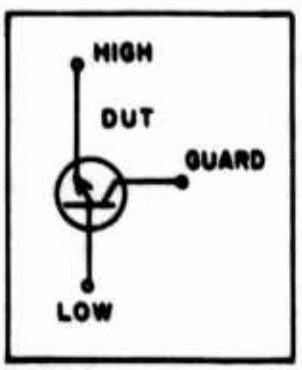

Fig. 3.3-13 Bridge connection of DUT for determination of base-emitter capacitance parameters

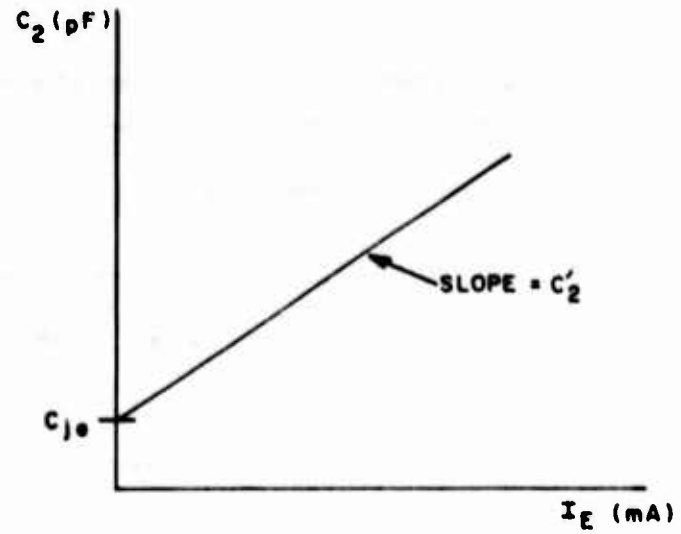

Fig. 3.3-14 Typical plot of C_2 vs $-I_E$

It is necessary to mention at this point that more detailed, complex and in general, more accurate techniques can be employed to obtain the parameters which account for the capacitive nonlinearities in the BJT model However, those techniques outlined in this section are both sufficient and accurate.

3.3.6 C_1 - Base-Emitter Capacitance, C_3 - Base-Collector and Overlap Capacitance

C_1 and C_3 are parasitic capacitances which account for the leads, bond wires and package of the BJT. These capacitances are actually external to the model for the BJT and play a significant role at high frequencies (i.e. above 100 MHz).

There is no direct means of evaluating each parasitic component separately. Approximate values can be obtained using techniques addressed by Fang[7] or by adjusting element values to obtain a best fit between measured and calculated data. When no data are available to determine values for C_1 and C_3, C_1 and C_3 may be set to zero.

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10. "RF Power Devices," RCA Solid State Databook SSD-205, RCA Corporation, 1972.

3.4 NCAP Junction Field-Effect Transistor Model Parameters

The RADC Nonlinear Circuit Analysis Program NCAP can be used to calculate nonlinear effects in electronic circuits containing Junction Field-Effect Transistors (JFET). In this section procedures for determining the NCAP n-channel JFET (n-JFET) model parameters will be given. Similar procedures can be used for p-channel JFETs. As a specific example the NCAP JFET model parameters will be determined for a 2N3823 n-JFET biased at V_{GS} = -1.557 V, V_{DS} = +15 V, and I_D = 40 μA. We first review the NCAP JFET analytic model. Then we describe the experiments performed to determine model parameters. We also discuss the data processing techniques used to obtain numerical values for the model parameters.

3.4.1 NCAP Total Equivalent Circuit for a JFET

The nonlinear device model used for the n-JFET shown in Fig. 3.4-1 is referred to as a total equivalent model.[1-3] The capacitors C1, C2, and C3 shown in Fig. 3.4-1 are constant extrinsic linear circuit elements. These capacitors are parasitic elements which have values in the 0.1 to 5 pF range. An intrinsic device model for the JFET is shown enclosed within dotted lines. The capacitor C_{GD} is the gate-drain capacitance which is modeled as a constant linear circuit element. The resistors R_S and R_D are the intrinsic source and drain resistances which result because the diffused gate region does

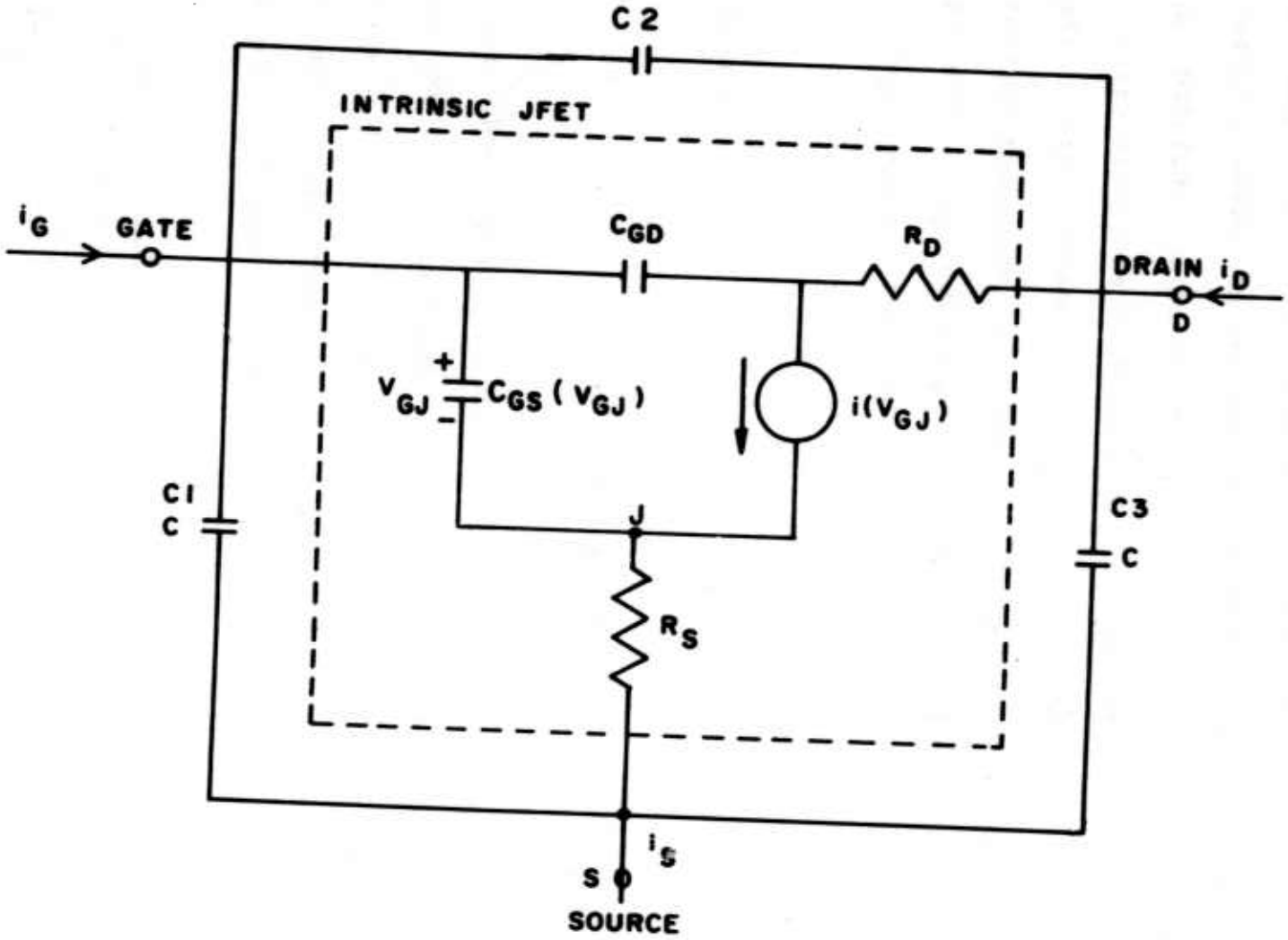

Fig. 3.4-1 Total equivalent circuit model for the n-JFET

not completely overlap the conducting channel and because the metallized source and drain contacts are not perfect short-circuits. These resistors are modeled as constant linear circuit elements. The resistor R_D is not actually included in the NCAP JFET model but can be inserted as an extrinsic circuit element. The two nonlinear circuit elements are the gate-source capacitance $C_{GS}(v_{GJ})$ and the dependent current generator $i(v_{GJ})$, where v_{GJ} is the voltage across C_{GS}. The DC voltage V_{GJ} is related to the actual DC terminal voltage V_{GS} by

$$V_{GJ} = V_{GS} - I_D R_S, \qquad (3.4\text{-}1)$$

where I_D is the DC drain current. The DC gate current I_G is assumed to be zero.

The computer program NCAP contains an analytic model for a JFET which is well-suited for nonlinear analysis. At DC the dependent current generator $i(v_{GJ})$ equals $I_{DSAT}(V_{GJ})$ where $I_{DSAT}(V_{GJ})$ is the DC drain current in the region where the DC drain current is independent of the DC drain voltage V_{DS}. The DC saturated drain current I_{DSAT} is given by

$$I_{DSAT} = \frac{3I_{D_{max}}}{2}^{\rho} \left[-\rho + \sqrt{\rho^2 + 4\left(\frac{1}{3} - \eta + \frac{2}{3}\eta^{1.5}\right)}\right], \qquad (3.4\text{-}2)$$

$$\eta = (V_{GJ} + \Psi) / (V_p + \Psi), \qquad (3.4\text{-}3)$$

$$\rho = (1 - \exp(-\Gamma)) / \Gamma^2, \qquad (3.4\text{-}4)$$

where Ψ is the built-in potential, V_p the gate-source cutoff voltage, and $I_{D_{max}}$ and Γ parameters. Equation (3.4-2) for I_{DSAT} contains four parameters ($I_{D_{max}}$, Γ(or ρ), Ψ, and V_p) which can be determined experimentally. Note that the voltages V_{GJ}, Ψ , and V_P are negative numbers for the n-JFET. Also note that either the parameter Γ or ρ may be used; however, as will be seen subsequently, it is simpler to use the parameter ρ.

The nonlinear gate-source capacitance C_{GS} is modeled using the expression

$$C_{GS}(V_{GJ}) = K [-V_{GJ} - V_o]^{-m}, \qquad V_{GJ} < 0 \qquad (3.4\text{-}5)$$

where K is a constant, V_o a built-in potential, and the exponent m a constant. Note that for the n-JFET both V_{GJ} and V_o are negative real numbers. We expect the built-in potential V_o to be in the range -0.5 to -0.7 V for a silicon n-JFET. The exponent m is 0.5 for an ideal abrupt pn junction and 0.333 for an ideal linearly graded pn junction. We anticipate a value for m in the range 0.3 to 0.5. Equation (3.4-5) contains three parameters K, V_o, and m which can be determined experimentally.

We may summarize the NCAP analytic model parameters in Table 3.4-1.

TABLE 3.4-1

NCAP JFET Analytic Model Parameters

V_{GS}	DC gate-source voltage
R_S	source resistance
C_{GD}	gate-drain capacitance
Ψ, V_p, Γ or ρ, $I_{D_{max}}$	parameters of $I(V_{GJ})$
K, m, V_O	parameters of $C_{GS}(V_{GJ})$
R_D, C1, C2, C3	extrinsic circuit elements (not intrinsic model parameters)

The designation of V_p as the pinch-off voltage in Refs. (2) and (3) is not standard. As used in NCAP V_p is equivalent to the gate-source cutoff voltage V_{GS}(cutoff) where V_{GS}(cutoff) is the value of V_{GS} that makes $I_D = 0$. The experimental procedures for measuring the model parameters will be given in the following sub-sections.

3.4.2 Experimental Methods for Determining the JFET Parameters, R_S, Ψ, V_p, $I_{D_{max}}$ and Γ (or ρ)

How NCAP JFET model parameter values are determined will be illustrated for the 2N3823 silicon n-channel JFET. Both DC and Audio Frequency (AF) measurement techniques are used to measure the five JFET parameters, R_S, Ψ, V_p, $I_{D_{max}}$ and Γ (or ρ). We

assume the built-in potential ψ lies in the range -0.5 to -0.7 V for a silicon n-JFET. We use an iterative procedure to determine V_p and R_S. First we obtain an approximate value for V_p experimentally. Next we determine a value for R_S experimentally. Then a value for V_p is determined using another experimental procedure. We also determine a set of values of I_{DSAT} versus V_{GS} from which final values for the parameters $I_{D_{max}}$, Γ (or ρ), and Ψ can be determined using a curve-fitting technique.

A DC experimental method is used to determine a value for R_S.[5] The JFET is operated in the linear region where the DC drain-source voltage V_{DS} is much less than $|V_p|$. The JFET equivalent circuit shown in Fig. 3.4-1 may also be used for DC analysis. For $V_{DS} << |V_p|$ we replace the current generator $i(V_{GJ})$ by a resistor $RQ1(V_{GJ})$ where

$$1/RQ1 = G_o [1 - \sqrt{n}\ ], \tag{3.4-6}$$

where G_o is the wide-open channel conductance.[6] Again we mention that the parameter V_p is the gate-source cutoff voltage. For $V_{DS} << |V_p|$ we define the resistance

$$R_{DSO} = V_{DS}/I_D = R_D + RQ1 + R_S. \tag{3.4-7}$$

Using Eqs. (3.4-3), (3.4-6), and (3.4-7) we obtain

$$R_{DSO} = (R_D + R_S) + G_o^{-1} X, \tag{3.4-8}$$

where

$$X = (1 - \sqrt{n}\ )^{-1}$$

By plotting experimental values for R_{DSO} versus values for X, we

can determine the sum $R_D + R_S$ from the intercept on the R_{DSO} axis.

Shown in Fig. 3.4-2 is the experimental system used to measure the resistance R_{DSO} of a 2N3823 silicon n-JFET. Conventional laboratory DC digital voltmeters and ammeters were used to measure V_{DS}, V_{GS} and I_D. Values of I_D were measured as a function of V_{GS} at V_{DS} = 0.1 V and at V_{DS} = 0.2 V, and values for R_{DSO} were calculated using Eq. (3.4-7). These values are given in Table 3.4-2 . The average value for R_{DSO} is also given.

TABLE 3.4-2

Values for R_{DSO} Measured at $V_{DS} << |V_p|$ for a 2N3823 n-JFET

V_{GS} V	$R_{DSO}(\Omega)$ at V_{DS} = 0.1 V	$R_{DSO}(\Omega)$ at V_{DS} = 0.2 V	$R_{DSO}(\Omega)$ average
0.0000	246	247	246
-0.200	281	278	279
-0.400	319	317	318
-0.600	370	377	374
-0.800	486	494	490
-1.000	658	690	674
-1.200	1176	1234	1205
-1.400	4762	4348	4555
-1.600	——	——	——

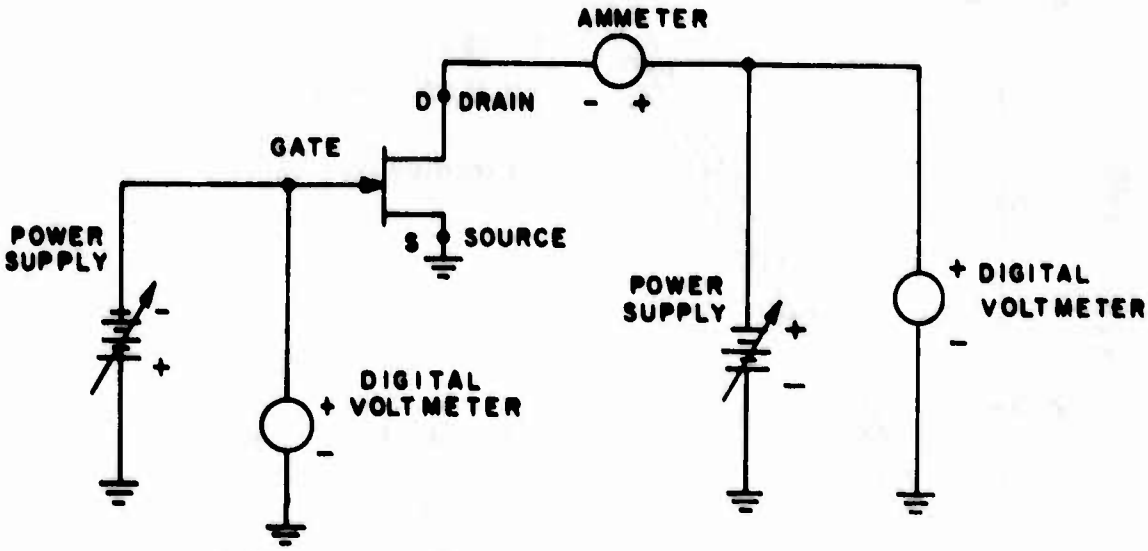

Fig. 3.4-2 Basic test circuit for measuring the n-JFET DC characteristics

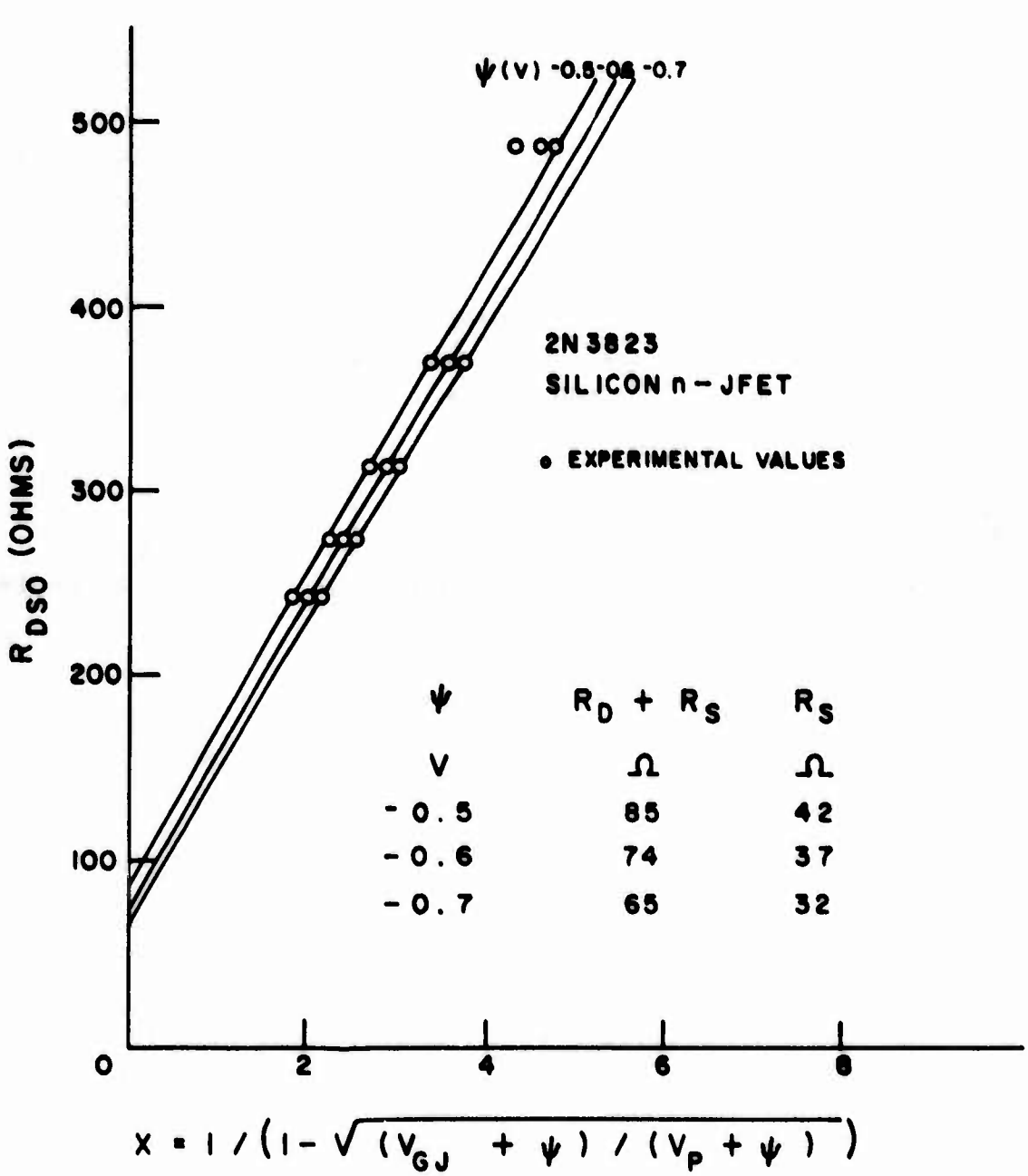

Fig. 3.4-3 Values of R_{DSO} versus X for several values of ψ using V_p = -1.70 V and $V_{GJ} = V_{GS}$

Shown in Fig. 3.4-3 are experimental values for R_{DSO} plotted versus calculated values for X. To calculate values for X, we use Eq. (3.4-3) and we assume that $V_{GJ} = V_{GS}$ which is equivalent to assuming that the $I_D R_S$ voltage drop is negligible (See Eq. (3.4-1)). Note that for $V_{DS} << |V_p|$, the I_D values are small, and the term $I_D R_S$ is also small. If subsequent calculations indicated that the $I_D R_S$ value was not negligible compared to V_{GS} , we would use an iterative calculation procedure. We determined an experimental value of -1.7 V for V_p by measuring the gate-source voltage V_{GS} that made I_{DSAT} less than 1 μA. Using $V_{GJ} = V_{GS}$, and $V_p = -1.70$ V, we calculated values for X for three values of the built-in potential Ψ. For values of X < 4, a straight line did pass through several data points for each value of Ψ as shown in Fig. 3.4-3 . Also given are the intercepts $R_D + R_S$ for these three values of Ψ . We assumed $R_S = R_D$ and $R_S = (R_S + R_D)/2$.[5] Values for R_S are also given in Fig. 3.4-3 . We observe that for Ψ in the range -0.5 to -0.7 V that R_S is in the range 32.5 to 42.5 Ω. We selected the intermediate value $R_S = 37$ Ω.

The experimental system shown in Fig. 3.4-2 was also used to measure DC values of I_{DSAT} versus V_{GS} . These values are given in Table 3.4-3 . The values given for I_{DSAT} are the values read on the ammeter corrected for the current through the digital VM used to measure V_{DS} . Also given in Table 3.4-3 are values for V_{GJ} calculated using Eq. (3.4-1) with $R_S = 37$ Ω.

The system shown in Fig. 3.4-4 was used to make audio-frequency (AF) measurements of the n-JFET incremental

transconductance g_m as a function of V_{GS}. By plotting g_m/I_{DSAT} vs V_{GJ}, the value for V_p can be checked. To make the g_m measurements an AF generator was connected as shown in Fig. 3.4-4. A dual channel AF voltmeter was connected to drain and gate nodes. When connected in this manner, the gain reading on the dual channel voltmeter is given by the product $(-g_m)(1\ k\Omega)$. During the AF gain measurements, the digital VM used to measure V_{DS} was disconnected. The AF gain measurements were made at an AF frequency of 1 kHz. The values for g_m are also given in Table 3.4-3.

TABLE 3.4-3

Values for I_{DSAT}, V_{GJ}, and g_m as a Function of V_{GS} at V_{DS} = 15 V and with R_S = 37 Ω

V_{GS}	I_{DSAT}	V_{GJ}	g_m
V	mA	V	mmho
0	4.3	-0.159	3.47
-.200	3.55	-0.331	3.38
-.400	2.85	-0.505	3.16
-.600	2.10	-0.678	2.85
-.800	1.55	-0.857	2.57
-1.000	0.967	-1.036	2.16
-1.200	0.535	-1.220	1.67

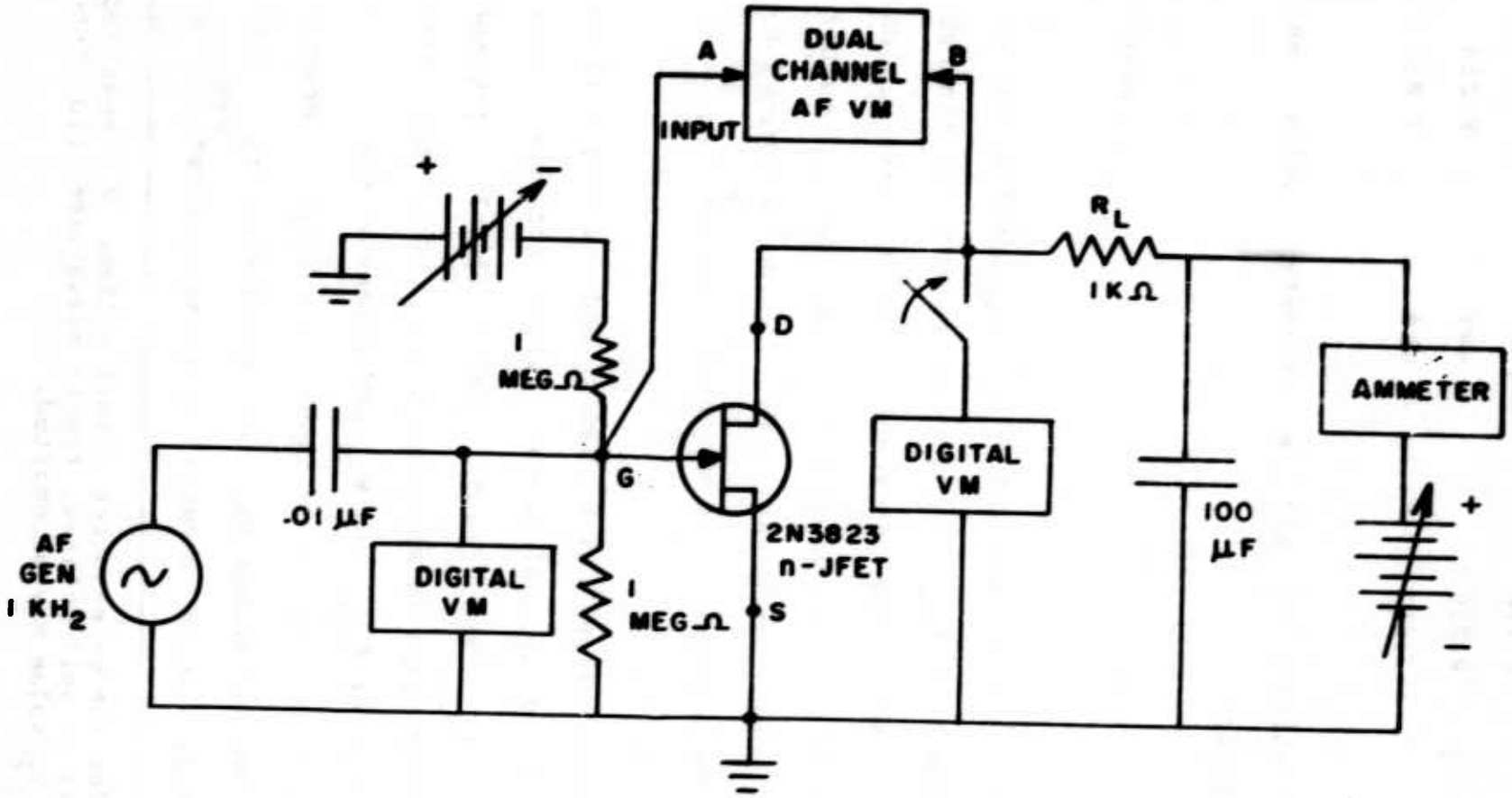

Fig. 3.4-4 AF test system used to measure n-JFET transconductance g_m

-1.400	0.170	-1.437	1.00
-1.600	0.019	-1.600	0.254
-1.700	0.003	-1.700	0.053

The pinch-off voltage V_p can be estimated using an approximate JFET relation

$$I_{DSAT}/g_m = -(V_p - V_{GJ}) / n, \qquad (3.4\text{-}9)$$

where n is a parameter.[2] Using the values for I_{DSAT} and g_m given in Table 3.4-3, values for I_{DSAT}/g_m were calculated and plotted versus V_{GJ} in Fig. 3.4-5 . The intercept on the V_{GJ} axis yields a value for V_p = -1.70 V. This value for the gate-source cutoff voltage V_p is in good agreement with a value determined by measuring the DC gate-source voltage V_{GS} that reduces I_{DSAT} to values less than 1 μA. (2)

Having determined values for V_p and R_S and assuming Ψ is in the range -0.5 to -0.7 V, we calculated values for the other unknown parameters $I_{D_{max}}$ and ρ (and Γ) in Eq. (3.4-2) using the computer program VJFET given in Appendix 3.4A. Using the data given in Table 3.4-3 for I_{DSAT} and V_{GS} and parameter values V_p = -1.7 V, R_S = 37 Ω, and Ψ = -0.5 V as inputs, the computer program VJFET yields many sets of values for the parameters $I_{D_{max}}$ and ρ (or Γ) as outputs. Using several of these computed sets of

(2) When the value for the gate-source cutoff voltage V_p measured using DC techniques is well defined, the AF measurement procedure used to check the V_p value may be omitted.

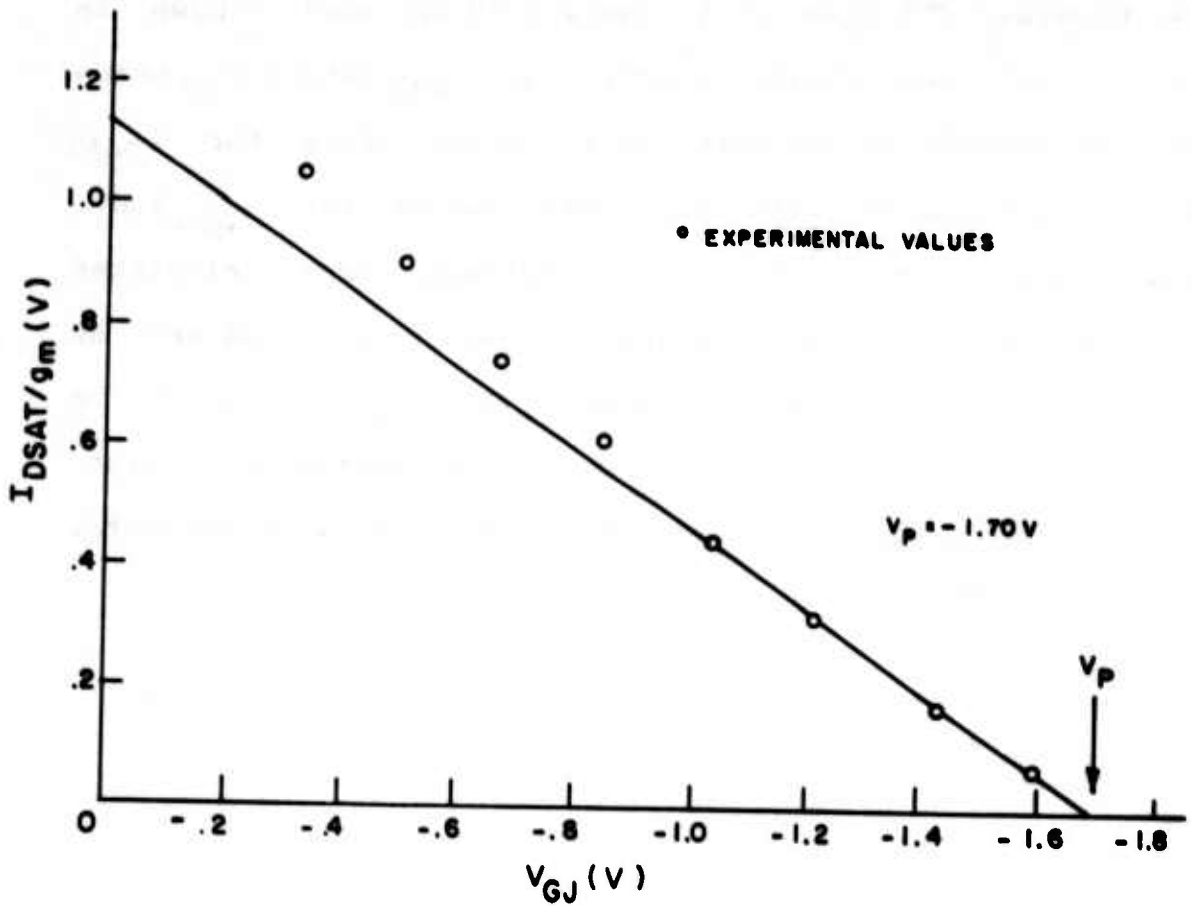

Fig. 3.4-5 Values of I_{DSAT}/g_m versus V_{GJ}. The data given in Table 3.4-3 are used to calculate values for I_{DSAT}/g_m

parameter values for $I_{D_{max}}$ and ρ (or Γ), values for I_{DSAT} versus V_{GS} were calculated using Eqs. (3.4-2)-(3.4-4). The interactive computer program WFET given in Appendix 3.4B was used. Shown in Fig. 3.4-6 are two calculated curves of I_{DSAT} versus V_{GS} which fit the experimental values quite well. Other values for I_{DSAT} versus V_{GS} calculated with different values for $I_{D_{max}}$ and ρ (or Γ) were also plotted, but curves through these calculated values did not fit the experimental values quite as well as curves 1 and 2. We observe that curve 1 with $I_{D_{max}}$ = 13.95 mA and ρ = 0.530 (Γ = 1.1303) appears to fit the experimental values better. These values will be used in the summary of parameter values given in Table 3.4-6.

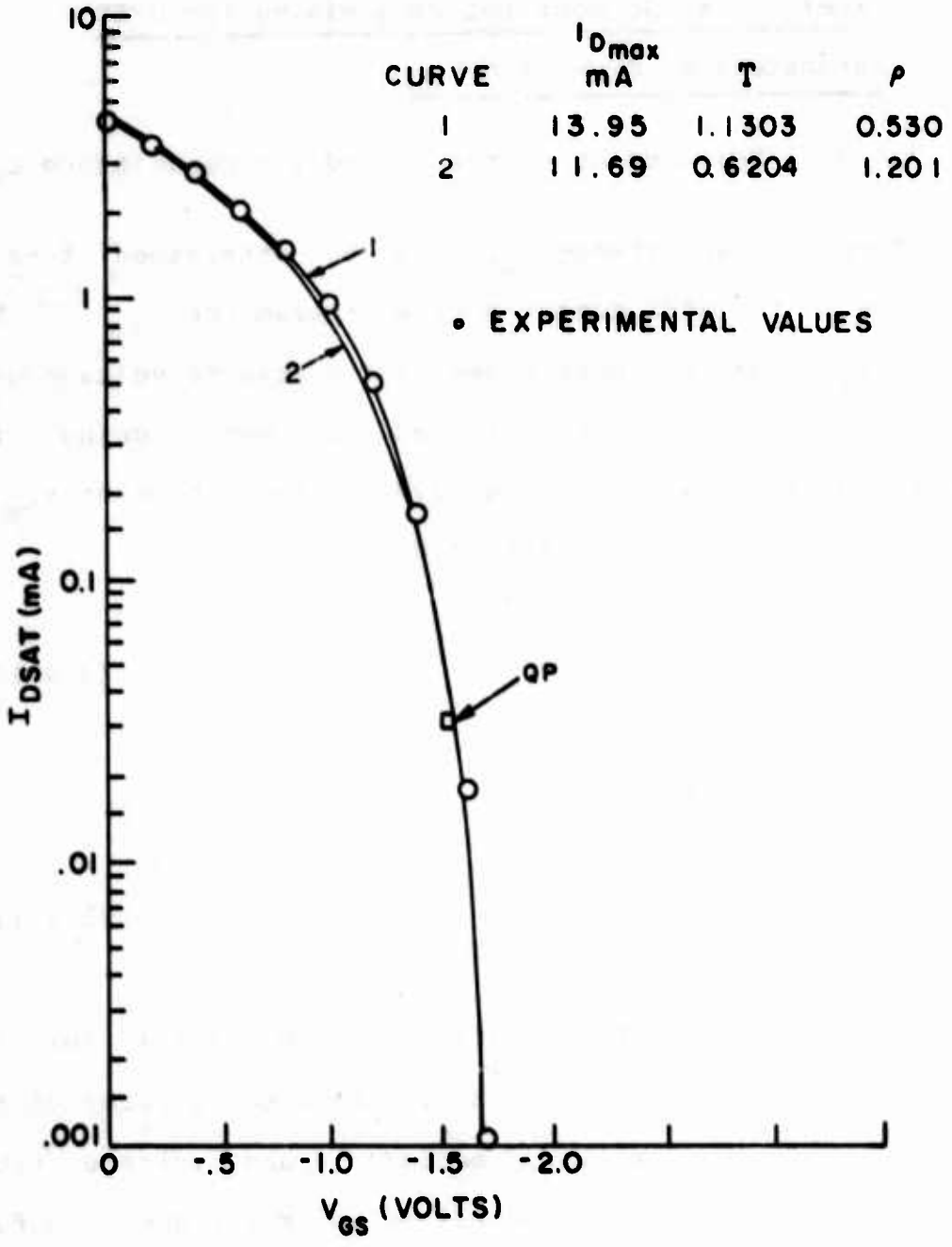

Fig. 3.4-6 Experimental and calculated values for I_{DSAT} vs V_{GS}. The calculated values for I_{DSAT} are obtained using Eqs. (3.4-2) and (3.4-4) with Ψ = -0.5 V, V_p = -1.7 V, R_S = 37 Ω, and with the parameters values for $I_{D_{max}}$ and ρ (or Γ) indicated

3.4.3 Experimental Methods for Determining the JFET Parameters K, m, V, and C_{GD}.

3.4.3.1 Measurement of the gate-drain capacitance C_{GD}

The gate-drain capacitance C_{GD} can be determined from a measured value of the JFET common-source y-parameter y_{rs}.[2,6] The y-parameter y_{rs} can be determined from a reverse voltage gain measurement. Such a measurement can be made using the experimental system shown in Fig. 3.4-7. The parameter y_{rs} at frequencies near 1 MHz may be expressed as

$$y_{rs} = -j\omega C_{rss} \qquad (3.4\text{-}10)$$

and the parameter C_{rss} is given by

$$C_{rss} = C2 + C_{GD}. \qquad (3.4\text{-}11)$$

Using the equivalent circuit given in Fig. 3.4-1 for the JFET, an expression for C_{rss} can be obtained in terms of the voltage gain A_v of the auxillary amplifier and voltage ratio V_B/V_A measured on the dual channel AC voltmeter shown in Fig. 3.4-7. This expression is

$$C_{rss} = \frac{3180\ \rho F}{f(MHz)} \times \frac{1}{A_v} \times \frac{V_B}{V_A}, \qquad (3.4\text{-}12)$$

where the signal generator frequency f is in MHz. Equation (3.4-12) is obtained by noting that when the reactance of the

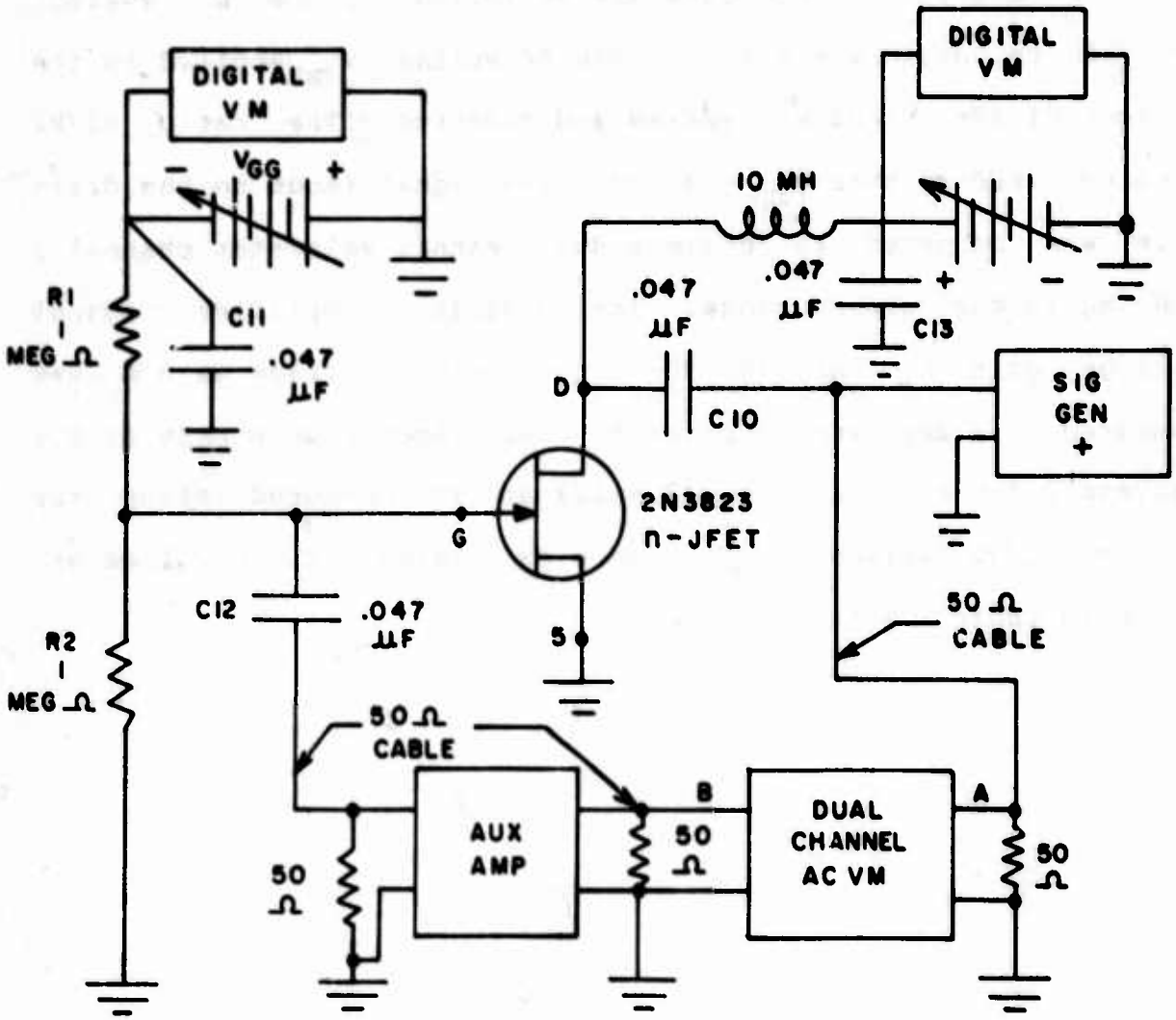

Fig. 3.4-7 Experimental system used to determine the gate-drain capacitance C_{GD}. The n-JFET reverse voltage gain is measured at frequencies near 1 MHz.

coupling capacitor C12 is much less than 50 Ω, the parallel capacitors C_{GD} and C2 (in the JFET model) and the 50 Ω resistor at the auxillary amplifier input form a voltage divider.

The measurement procedure was as follows. The DC voltage applied to drain was + 15 V. The DC voltage V_{GG} applied to the voltage divider R1/R2 was varied and measured. The ratio R1/R2 equaled 1.000 so that $V_{GS} = V_{GG}/2$. The signal input to the drain node was adjusted to obtain a dual channel voltmeter channel B reading in the correct range. The auxillary amplifier nominal voltage gain A_V was 40 dB· the actual voltage gain A_V was measured in a separate experiment. Measurements were made at 0.5 MHz and 2.0 MHz. Using Eq. (3.4-12) and the measured values for A_V and V_B/V_A, values for C_{rss} were calculated. These values are given in Table 3.4-4.

TABLE 3.4-4

Values for C_{rss} versus V_{GS} for a 2N3823 JFET
Measured at 0.5 MHz and 2.0 MHz[a]

V_{GS} ($V_{GG}/2$)	$C_{rss} = C2 + C_{GD}$ at 0.5 MHz	at 2.0 MHz
Volts	pF	pF
-0.016	0.98	0.94
-0.500	0.90	0.88
-1.000	0.88	0.84
-1.500	0.87	0.82
-2.000[b]	0.88	0.82
-3.000[b]	0.87	0.82

(3)

We cannot separate C2 from C_{GD} using this measurement technique. We set C2 = 0 and $C_{GD} = C_{rss}$ at the QP value of V_{GS}. In the example used in this section, the QP values are V_{GS} = -1.577 V, V_{DS} = +15 V, and I_D = 40 µA. The larger value of C_{GD} at the QP is 0.87 pF. The value C_{GD} = 0.87 pF includes the actual value of C_{GD} plus parasitic capacitances between the gate lead and drain lead due to the socket and wiring. This value is given in the summary of 2N3823 JFET parameter values in Table 3.4-6.

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(3)

a The JFET is being operated with V_{DS} = + 15 V.

b The JFET is cutoff with V_{GS} < -1.70 V.

An alternate method for measuring the gate-drain capacitance C_{GD} is illustrated in Fig. 3.4-8. Although this method was not used for the 2N3823 n-JFET being used as an example in this section, it has been used successfully with other 2N3823 n-JFETs. The measurement method illustrated in Fig. 3.4-8 provides a direct measurement of the capacitance C_{GD} on the 1 MHz capacitance bridge. This is a significant advantage.

3.4.3.2 Measurement of the gate-source capacitance parameters K, V_o, and m

The gate-source capacitance C_{GS} can be determined from a measured value of the JFET common-source y-parameter y_{is}.[2,6] The y-parameter y_{is} can be determined from an input admittance measurement. The parameter y_{is} at frequencies near 1 MHz may be expressed as

$$y_{is} = G_{iss} + j\omega C_{iss}, \qquad (3.4\text{-}13)$$

and the parameter C_{iss} is given by

$$C_{iss} = C1 + C2 + C_{GD} + C_{GS}, \qquad (3.4\text{-}14)$$

where C1, C2, C_{GD} and C_{GS} are the JFET model parameters shown in Fig. 3.4-1.

The test circuit for measuring C_{iss} is shown in Fig. 3.4-9. A 0.047 μF capacitor was connected from node D to node S. This capacitor acts as a short-circuit at 1 MHz and connects the drain and source of the JFET. A 15 V DC power supply provides the

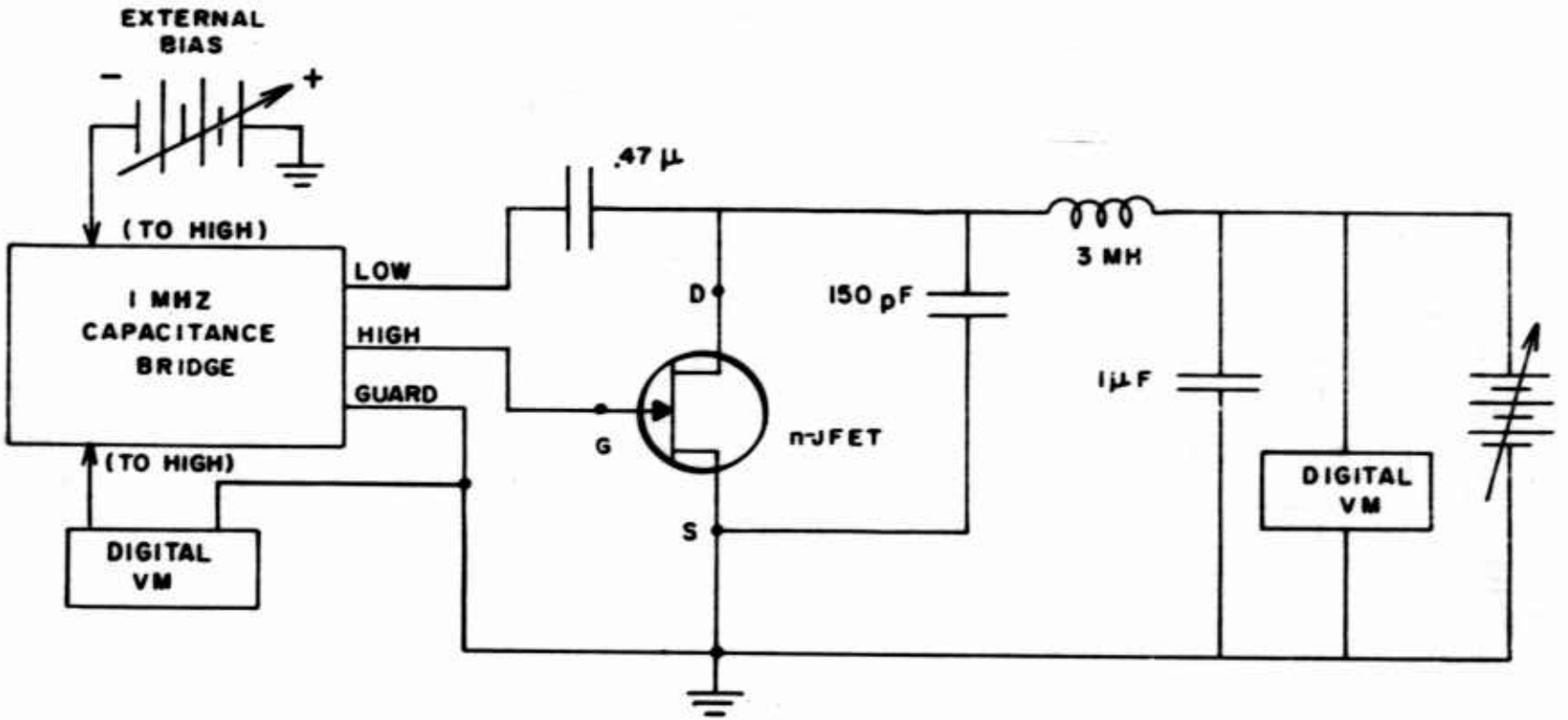

Fig. 3.4-8 Test circuit for measuring C_{rss}. The 1 MHz capacitance bridge can be biased externally, and the external bias at the high terminal can be monitored with an external voltmeter as shown.

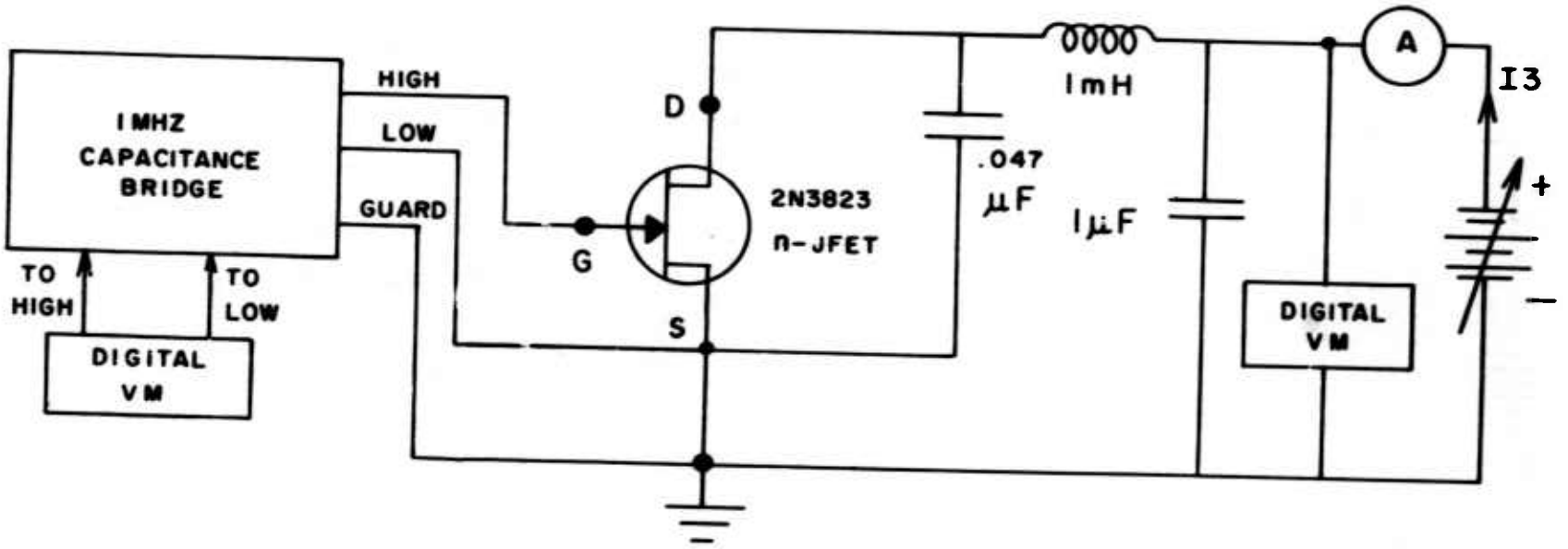

Fig. 3.4-9 Test circuit for measuring C_{iss}. The 1 MHz capacitance bridge contains an internal bias supply which can be used to control V_{GS}. The V_{GS} value is read on an external digital voltmeter.

drain bias. The drain power supply DC current was measured with an ammeter. A 1 MHz capacitance bridge was used to make input admittance measurements. Connections were made from the capacitance bridge to the gate of the 2N3823 JFET and to the signal ground. The capacitance bridge contains an internal DC power supply which was used to provide the gate-source bias voltage V_{GS}. A digital voltmeter was connected to the terminals on the capacitance bridge provided for monitoring this DC voltage. Input admittance measurements were made using the balanced mode method described in the capacitance bridge instruction manual. The measured values are given in Table 3.4-5.

TABLE 3.4-5

Measured Values of V_{GS}, I3, and C_{iss} and Derived Values of V_{GJ}, I_D and $C_{iss} - C_{GD} - C2$ for the 2N3823 n-JFET.

V_{GS} Volts	I3 mA	C_{iss} pF	I_D mA	V_{GJ} Volts	$C_{iss} - C_{GD} - C2$ pF
-0.000	2.96	4.31	2.95	-0.109	3.44
-0.104	2.66	4.15	2.65	-0.202	3.28
-0.202	2.36	4.02	2.35	-0.289	3.15
-0.302	2.16	3.97	2.15	-0.382	3.10
-0.406	1.86	3.88	1.85	-0.474	3.01
-0.501	1.66	3.78	1.65	-0.562	2.91
-0.602	1.46	3.74	1.45	-0.656	2.87
-0.802	1.06	3.58	1.05	-0.841	2.71
-1.002	0.66	3.51	.65	-1.026	2.64
-1.250	0.265	3.37	.250	-1.259	2.50
-1.504	0.065	3.22	.050	-1.506	2.35
-1.754[a]	0.015[b]	3.08	.000	-1.754	2.21
-2.005[a]	0.015[b]	2.97	.000	-2.005	2.10
-2.517[a]	0.015[b]	2.83	.000	-2.517	1.96
-3.009[a]	0.015[b]	2.72	.000	-3.009	1.85
-4.002[a]	0.015[b]	2.60	.000	-4.002	1.73
-5.001[a]	0.015[b]	2.50	.000	-5.001	1.63

(4)

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(4)

a The 2N3823 n-JFET is cutoff for $V_{GS} < -1.70$ V.

b The voltmeter current is .015 mA.

The data presented in Table 3.4-5 can be used to obtain values for the parameters K, V_o, and m in the $C_{GS}(V_{GJ})$ expression which is Eq. (3.4-5). First the DC voltage V_{GJ} was calculated using Eq. (3.4-1) with R_S = 37 Ω. The values for I_D were calculated by subtracting 0.015 mA from the values for the drain DC bias supply current I3 given in Table 3.4-5 since I3 equaled 0.015 mA when the 2N3823 JFET was cutoff. These values for I_D do differ slightly from the values for I_{DSAT} given in Table 3.4-3, but the differences do not significantly affect the V_{GJ} calculation. Next, we subtract the known value of C2 + C_{GD} (0.87 pF) from the C_{iss} values to obtain values for C_{iss} - C2 - C_{GD}. The values for I_D, V_{GJ}, and C_{iss} - C_{GD} - C2 derived from the measured values for I3, V_{GS} and C_{iss} are also given in Table 3.4-5 for a 2N3823 n-JFET.

Using Eqs. (3.4-5) and (3.4-14), we obtain the expression

$$C_{iss} - C2 - C_{GD} = C1 + K|V_{GJ} + V_o|^{-m}, \qquad (3.4\text{-}15)$$

which now must be fitted to the values of C_{iss} - C2 - C_{GD} versus V_{GJ}. We know the value for V_o lies in the range -0.5 to -0.7 V and the value for m lies in the range 0.3 to 0.5 for a silicon JFET. We use as initial trial values V_o = -0.5 V and m = 0.5 (the value for an abrupt pn junction gate). Having chosen initial values of V_o = -0.5 V and m = 0.5, the next step is to select two sets of values for C_{iss} - C2 -C_{GD} and V_{GJ} (with V_{GJ} > V_p = -1.7 V) and to solve Eq. (3.4-15) for C1 and K. Using the values C_{iss} - C2 - C_{GD} = 3.44 pF at V_{GJ} = -0.019 V and C_{iss} - C2

- C_{GD} = 2.51 pF at V_{GJ} = -1.754 V (the closest value to $V_{GS} = V_p$), we obtained C1 = 0.80 pF and K = 2.13 pF - $V^{.5}$. How well these initial choices for V_o, m, C1 and K fit the data can be determined by plotting the values of $C_{GS} = C_{iss} - C2 - C_{GD} - C1$ versus values of $|V_{GJ} + V_o|$ on log-log paper and drawing a straight line of slope - m through these values. Shown in Fig. 3.4-10 is such a plot for the parameter values C2 + C_{GD} = 0.87 pF, C1 = 0.80 pF and V_o = -0.5 V. A straight line with slope = -0.50 fits the plotted values very well for $V_{GS} > V_p$. (Equation (3.4-15) applies when the JFET is not cutoff.) The value of the parameter K for the straight line plotted in Fig. 3.4-10 is 2.20 pF - $V^{.5}$ which is within 5 percent of the value calculated previously. We could use either value. Since the initial choices for V_o, m, C1 and K fit the C_{iss} versus V_{GJ} data quite well, no additional effort was made to fit other values of V_o, m, C1, and K to the C_{iss} versus V_{GJ} data. The parameter values V_o = -0.5 V, m = 0.5, C1 = 0.80 pF, and K = 2.20 pF-$V^{.5}$ are given in the summary of the 2N3823 JFET parameter values in Table 3.4-6.

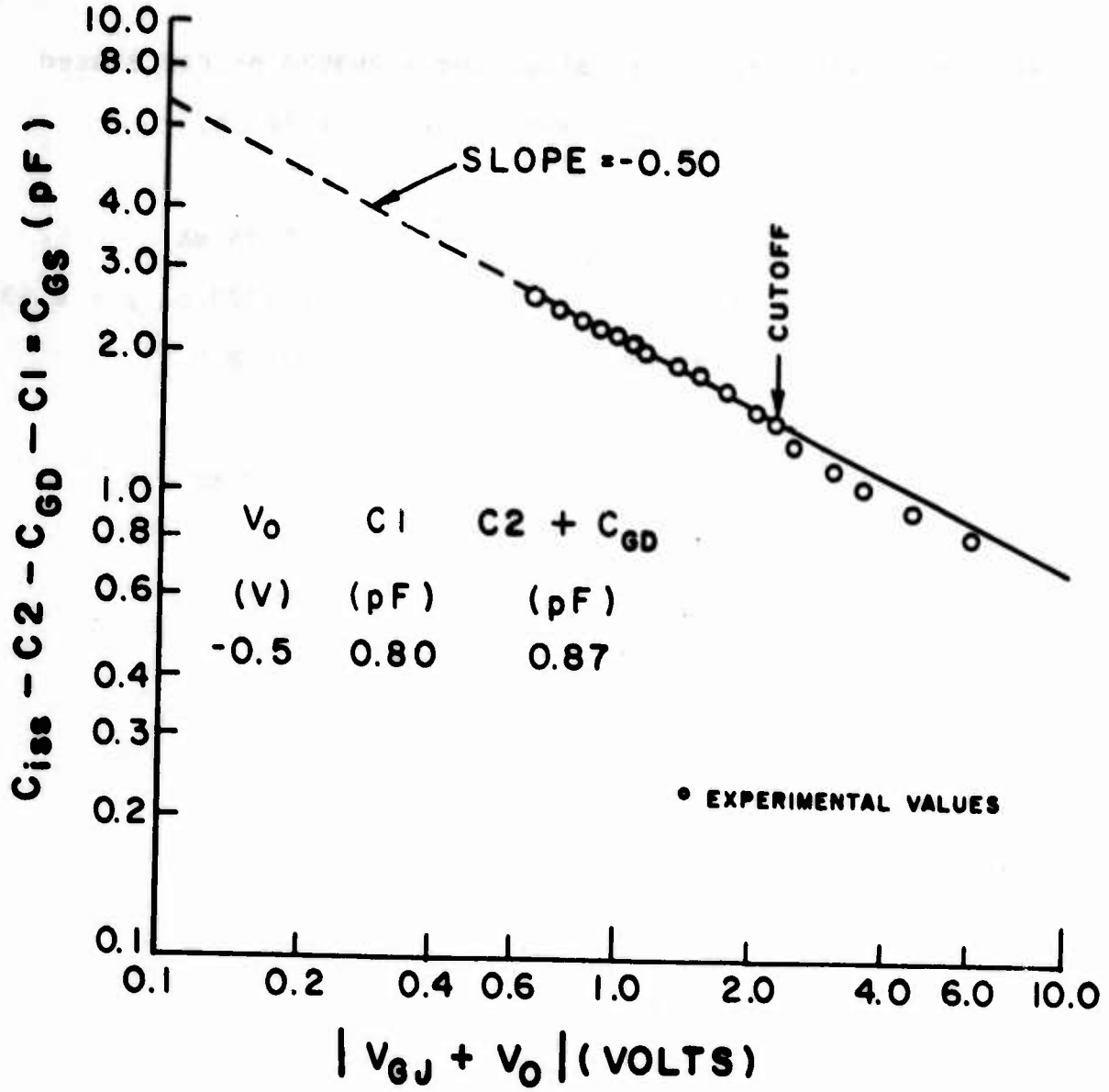

Fig. 3.4-10 Values of C_{GS} versus $|V_{GJ} + V_O|$. Values for C_{iss} and V_{GJ} are taken from table 5. Equation (3.4-1) with R_s = 37 Ω is used to calculate values for V_{GJ}

TABLE 3.4-6

NCAP Analytic Model Parameter Values for a 2N3823 n-JFET Biased at V_{GS} = -1.577V, V_{DS} = +15 V, and I_D = 40 μA.

V_{GS}	= - 1.557 V	$I_{D_{max}}$	= 13.95 mA
R_S	= 37 Ω	Γ	= 1.1303 or ρ = 0.530
C_{GD}	= 0.87 pF	V_p	= -1.70 V
R_D	= R_S = 37 Ω	Ψ	= -0.5 V
C1	= 0.8 pF	K	= 2.20 pF - $V^{.5}$
C1	= 0	m	= 0.5
C3	= 0	V_o	= -0.5 V

Appendix 3.4A

VJFET Program for Determining $I_{D_{max}}$ and ρ (or Γ) from Measured Values of I_{DSAT} and V_{GJ}

```
100 DIMENSION CUR(9),VOLT(9)
110C   ORDER PAIRS OF CURRENT AND VOLTAGE
120 DATA CUR/4.30,3.60,2.83,2.10,1.52,0.96,0.50,0.177,0.018/
130 DATA VOLT/.00,-.20,-.40,-.60,-.80,-1.0,-1.2,-1.4,-1.6/
140C  INPUT PARAMETERS
150 PRINT "VPI"
160 READ:VP
170 PRINT:"RHO"
180 READ RHO
190 PRINT "VBI"
200 READ VBI
210C*************************************************************
220 DO 110 J = 1,8
230 PRINT 1
240 KST = 1 + J
250 DO 110 K = KST,9
260 AID1 = CUR(J)*.001
270 AID2 = CUR(K)*.001
280 VG1 = VOLT(J) - CUR(J)*.037
290 VG2 = VOLT(K) -CUR(K)*.037
300 PRINT 1,VG1,AID1,VG2,AID2
310 VP = -1.7
320 DO 100 I = 1,100
330 A1 = AM(RHO,VG1,VP,VBI)
340 A2 = AM(RHO,VG2,VP,VBI)
350 B1 = DMDR(RHO,VG1,VP,VBI)
360 B2 = DMDR(RHO,VG2,VP,VBI)
370 FPR = -(A2*B1 -A1*B2)/(A2*A2)
380 ERROR = +AID1/AID2 -A1/A2
390 IF(ABS(ERROR).LT.0.0001) GO TO 105
400 EOFPR = ERROR/FPR
410 IF((RHO -EOFPR).LT.0.0) EOFPR=RHO/2.
420 100 RHO = RHO -EOFPR
430 105 CUR1 = AID1/3./RHO/A1
440     CUR2 = AID2/3./RHO/A2
450 110 PRINT 1,CUR1,CUR2,ERROR,FLOAT(I),RHO
460  1  FORMAT(1X,9G12.4)
470 STOP
480 END
```

```
490C ***************************************************************
500 FUNCTION AM(RHO,VG,VP,VBI)
510 A = (VG +VBI)/(VP +VBI)
520 B = 1./3. - A + 2.*(A**1.5)/3
530 AM = -RHO/2. +SQRT(RHO*RHO+4.*B)/2.
540 RETURN
550 END
560C***************************************************************
570 FUNCTION DMDR(RHO,VG,VP,VBI)
580 A = (VG +VBI)/(VP +VBI)
590 B = 1./3.-A +2.*(A**1.5)/3.
600 DMDR = -0.5 + RHO/SQRT(RHO*RHO + 4.0*B)/2.0
610 RETURN
620 END
```

Appendix 3.4B

JFET Program for Calculating Values of I_{DSAT} vs V_{GS}.

```
100 DIMENSION CUR(10),VOLT(10)
110 REAL ID1,ID2,IDMAX,IDMX1,IDMX2
120 CNST(X) = 4.*((1./3.-(X+VBI)/(VP+VBI))+(2./3.)*((X+VBI)/(VP+
130&           VBI))**1.5)
140 V(Y) =.5*(-RHO + (RHO*RHO +4.*((1./3.-(Y+VBI)/(VP+VBI)) +
150&       (2./3.)*((Y+VBI)/(VP+VBI))**1.5))**.5)
160 9 PRINT "NUMBER OF PAIRS"
170 READ 1,NN
180 PRINT:"CURRENT VALUES IN MA"
190 READ 1,CUR
200 PRINT:"VOLTAGE VALUES IN VOLTS"
210 READ 1,VOLT
220 PRINT:"SOURCE RESISTANCE IN K OHMS"
230 READ 1,RES
240 PRINT:"PINCH-OFF VOLTAGE IN VOLTS"
250 READ 1,VP
260 PRINT:"BUILT-IN VOLTAGE IN VOLTS"
270 READ 1,VBI
280 GAMMA = .5
290 N = NN - 1
300************************************************************
310 DO 2 I = 1,N
320 PRINT 11
330 ID1 = CUR(I)*.001
340 VG1 = VOLT(I) - CUR(I)*RES
350 PRINT:"          VG1          IDS1"
360 PRINT 7,I,VG1,ID1
370 PRINT 12
380 PRINT 6
390 KST = I + 1
400 DO 3 J = KST,NN
410 ID2 = CUR(J)*.001
420 VG2 = VOLT(J) - CUR(J)*RES
430 RATIO = ID1/ID2
440 X = 2.*RATIO*(RATIO - 1.)
450 Y = RATIO*RATIO*CNST(VG2) - CNST(VG1)
460 A1 = X*(2.*Y-X*CNST(VG2))
470 A2 = Y*Y
```

```
480 IF((-A2/A1).GE.0) GOTO 5
490 PRINT:"RHO IS IMAGINARY"
500 GOTO 3
510 5 CONTINUE
520*************************************************************
530 RHO = SQRT(-A2/A1)
540 IDMX1 = ID1/(3.*RHO*V(VG1))
550 IDMX2 = ID2/(3.*RHO*V(VG2))
560 DO 8 L = 1,1000
570 X = GAMMA
580 GAMMA = SQRT((1-EXP(-GAMMA))/RHO)
590 ERROR = 10.**(AINT(ALOG10(ABS(GAMMA)))-6.)
600 IF(ABS(GAMMA-X).LT.ERROR) GOTO 10
610 8 CONTINUE
620 PRINT:"GAMMA IS UNDERTERMINED AFTER 1000 ITERATIONS"
630*************************************************************
640 10 PRINT 7,J,VG2,ID2,IDMX1,RHO,GAMMA
650 3 CONTINUE
660 2 CONTINUE
670 PRINT:" ":PRINT:" ":PRINT:" ":PRINT:" "
680 PRINT:"AGAIN (YES=1  NO=0)"
690 READ 1,I
700 IF(I.EQ.1) GOTO 9
710 1 FORMAT(V)
720 6 FORMAT(9X,3HVG2,8X,4HIDS2,10X,6HIDSMAX,9X,3HRHO,10X,5HGAMMA)
730 7 FORMAT(1X,I2,3X,F8.4,3X,F10.7,3X,E13.6,3X,F9.6,3X,E13.6)
740 11 FORMAT(1X,70(1H-))
750 12 FORMAT(1X,13(2H *))
760 STOP:END
```

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4. R. B. Fair, "Harmonic Distortion in the Junction Field-Effect Transistor with Field Dependent Mobility," IEEE Trans. Electron Devices, Vol. Ed-19, pp. 9-13. January 1972.

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ILLUSTRATIONS

Figure 3.4-9 Test circuit for measuring C_{iss}. The 1 MHz capacitance bridge contains an internal bias supply which can be used to control V_{GS}. The V_{GS} value is read on an external digital voltmeter.

Figure 3.4-10 Values of C_{GS} versus $|V_{GJ} + V_o|$. Values for C_{iss} and V_{GJ} are taken from Table 3.4-5. Equation (3.4-1) with $R_S = 37\Omega$ is used to calculate values for V_{GJ}.

3.5 Vacuum Tube Diode

There are still many communication systems in use that use vacuum tubes. The Nonlinear Circuit Analysis Program NCAP can be used to calculate nonlinear effects in electronic circuits containing vacuum tube diodes, triodes, and pentodes. In this section procedures for determining the NCAP vacuum tube diode model parameters will be given.

3.5.1 NCAP Model For the Vacuum Tube Diode

The nonlinear device model used for the vacuum tube diode shown in Fig. 3.5-1 is referred to as a total equivalent model. The capacitor C_{pk} is the plate-to-cathode capacitance and the resistor R_D is the nonlinear plate-to-cathode resistance. It is assumed that the vacuum tube diode is operated at values of

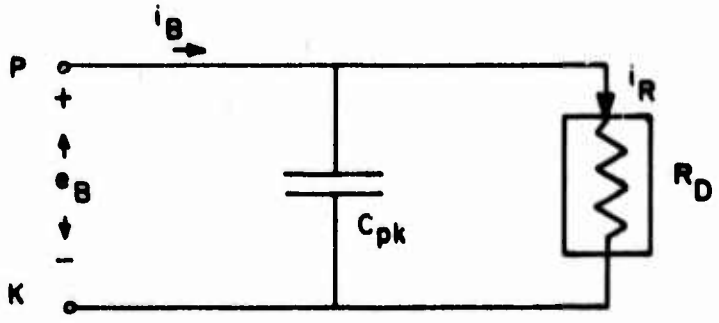

Fig. 3.5-1 Total equivalent circuit for the vacuum tube diode.

total instantaneous plate-cathode voltage e_B low enough so that the total instantaneous plate current i_B is spaced-charge limited

so that

$$i_R = Ge_B^{1.5} \qquad e_B > 0 \qquad (3.5\text{-}1)$$

where G is the perveance. The perveance G does depend upon the cathode heater current and the age of the tube, but it is assumed to be independent of the plate voltage e_B. The NCAP vacuum tube diode parameters are summarized in Table 3.5-1.

TABLE 3.5-1

NCAP Vacuum Tube Diode Model Parameters

Parameter	Description
G	Perveance
E_B	DC plate-cathode voltage at operating point
C_{pk}	Plate-to-cathode interelectrode capacitance

3.5.2 Determining the Vacuum Tube Diode Parameters G and E_B

The vacuum tube diode perveance G can be determined from the diode dc plate current I_B vs dc plate-cathode voltage E_B characteristics. An experimental system for measuring the I_B - E_B characteristics of a 6H6 vacuum tube diode (dual diode) is

shown in Fig. 3.5-2. Typical I_B - E_B characteristics are shown in Fig. 3.5-3.

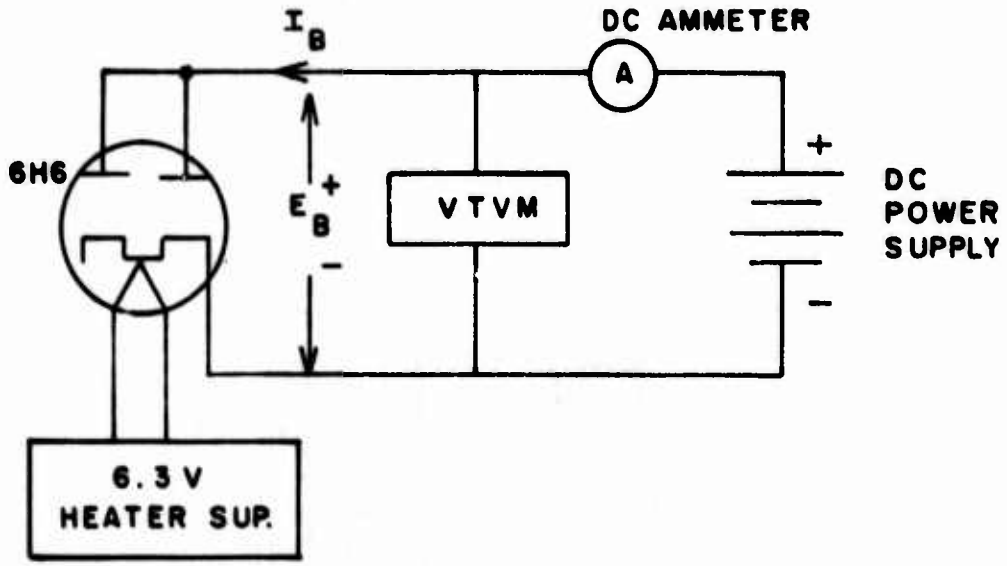

Fig. 3.5-2. Experimental system for measuring the 6H6 (dual vacuum tube diode) I_B - E_B characteristics.

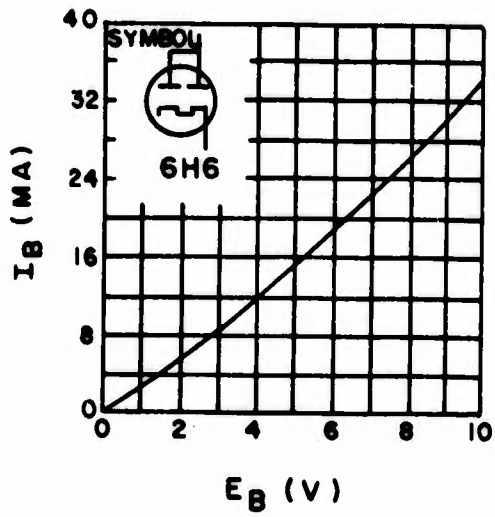

Fig. 3.5-3. Typical dc plate current vs plate-cathode voltage characteristics for the 6H6 vacuum tube diode. (From K. R. Spangenberg, "Vacuum Tubes," p. 5, McGraw Hill, New York, 1948.)

Using the data shown in Fig. 3.5-3 and Eq. (3.5-1), values for the ratio $I_B/E_B^{1.5}$ were calculated. These values are given in Table 3.5-2. It is seen that values for the ratio $I_B/E_B^{1.5}$ and hence the perveance G are not constant but decrease as the dc plate current I_B increases. Over the current range

TABLE 3.5-2

Values of Perveance G vs DC Plate Current I_B

For a 6H6 Vacuum Tube Diode

I_B (A)	E_B (V)	$G = I_B(A)/E_B(V)^{1.5}$ $(A/V^{1.5})$
.004	1.5	.00217
.008	2.8	.00171
.012	4.1	.00145
.016	5.3	.00131
.020	6.3	.00126
.024	7.4	.00119
.028	8.5	.00113
.032	9.6	.00106

12 to 32 mA the perveance G has a value .00126 $A/V^{1.5}$ $\pm$ 16%.

The recommended procedure for selecting a value for the perveance G is to determine the vacuum tube diode dc operating point (I_B, E_B) and to calculate G using $G = I_B\,(A) \div E_B\,(V)^{1.5}$.

For example for a 6H6 vacuum tube diode having a dc operating point I_B = 24 mA and E_B = 7.4 V, the appropriate NCAP vacuum tube diode model parameter values are:

E_B = 7.4 V

G = .00119 $A/V^{1.5}$

3.5.3 Determining the Vacuum Tube Diode Parameter C_{pk}

An examination of data provided by manufacturers of vacuum tube diodes indicates that a value for the plate-to-cathode capacitance C_{pk} is not always provided. If that is the case, the capacitance C_{pk} can be measured directly on a 1 MHz capacitance bridge. The first step is to connect the appropriate terminals of the vacuum tube socket to the capacitance bridge and to null the capacitance bridge or to record the capacitance reading without the vacuum tube diode inserted in the socket. Then the vacuum tube diode is inserted in the socket, but the cathode heater is not connected (cold cathode). The increase in capacitance yields a value for one interelectrode capacitance combination. By measuring several interelectrode capacitance combinations, it is usually possible to estimate the interelectrode capacitance between two specific electrodes such as plate and cathode. An example will be given to illustrate how this can be accomplished.

When manufacturer's data are available, their use is recommended. For example the following capacitance data are provided in the RCA Receiving Tube Manual for the 6AL5 vacuum tube diode. The 6AL5 twin diode is widely used as a detector in FM and television circuits. The data provided are:

Direct Interelectrode Capacitances:

P* No. 1 to C* No. 1, Heater, and Internal Shield	2.5×10^{-12} F
P No. 2 to C No. 2, Heater, and Internal Shield	2.5×10^{-12} F
C No. 1 to P No. 1, Heater, and Internal Shield	3.4×10^{-12} F
C No. 2 to P No. 2, Heater, and Internal Shield	3.4×10^{-12} F
P No. 1 to P No. 2	$.07 \times 10^{-12}$ F

* P = Plate
C = Cathode

A simple model illustrating the major interelectrode capacitances for the 6AL5 twin diode is shown in Fig. 3.5-4.

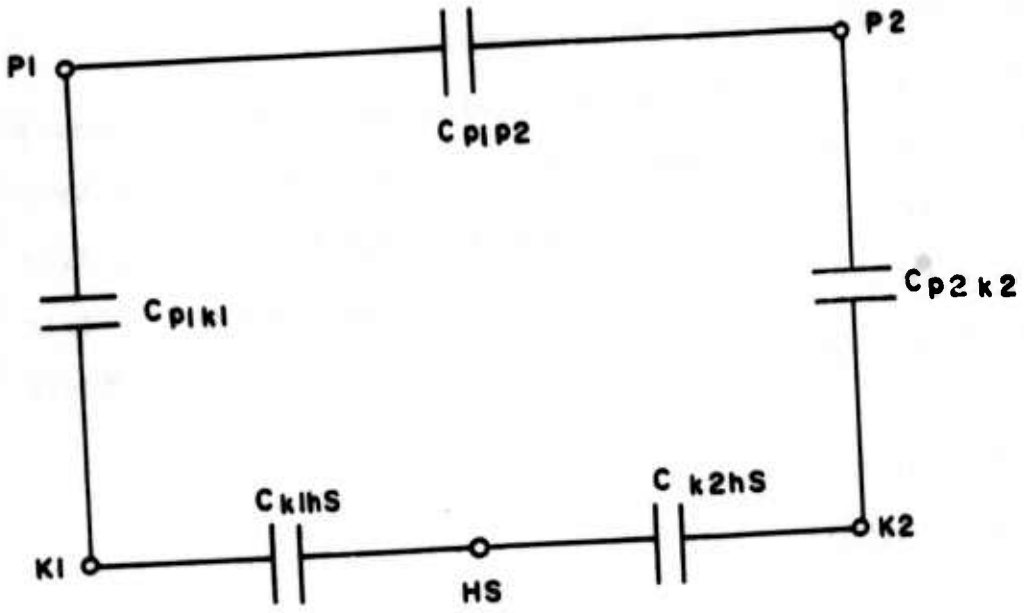

Fig. 3.5-4. Simple interelectrode model for a dual diode vacuum tube such as the 6AL5.

Using the direct interelectrode capacitance values, the interelectrode capacitance values given in Table 3.5-3 were determined.

TABLE 3.5-3

Values For the Interelectrode Capacitances

C_{p1k1}	Plate No. 1 to Cathode No. 1	2.5×10^{-12} F
C_{p2k2}	Plate No. 2 to Cathode No. 2	2.5×10^{-12} F
C_{p1p2}	Plate No. 1 to Plate No. 2	$.07 \times 10^{-12}$ F
C_{k1hs}	Cathode No. 1 to Heater-Shield	$.9 \times 10^{-12}$ F
C_{k2hs}	Cathode No. 2 to Heater-Shield	$.9 \times 10^{-12}$ F

The values for the plate-cathode interelectrode capacitances C_{p1k1} and C_{p2k2} can be entered as part of the set of NCAP parameter values for the vacuum tube diode. The other interelectrode capacitances must be specified separately as extrinsic (passive) components. It is important to note that other parasitic capacitances such as these associated with the tube socket and leads connected to the socket terminals may be important at frequencies greater than 100 MHz. Important parasitic capacitances can also be specified separately as extrinsic (passive) components.

3.6 Vacuum Tube Triode

The Nonlinear Circuit Analysis Program NCAP can be used to calculate nonlinear effects in electronic circuits containing vacuum tube triodes. In this section procedures for determining the NCAP vacuum tube triode model parameters will be given.

3.6.1 NCAP Model For the Vacuum Tube Triode

The nonlinear device model used for the vacuum tube triode shown in Fig. 3.6-1 may be called a total equivalent model. The interelectrode capacitors C_{gk}, C_{pg}, and C_{pk} are defined in Table 3.6-1. The triode space-charge current $g(e_G, e_B)$ depends upon the total instantaneous grid-cathode voltage e_G and total instantaneous plate-cathode voltage e_B.

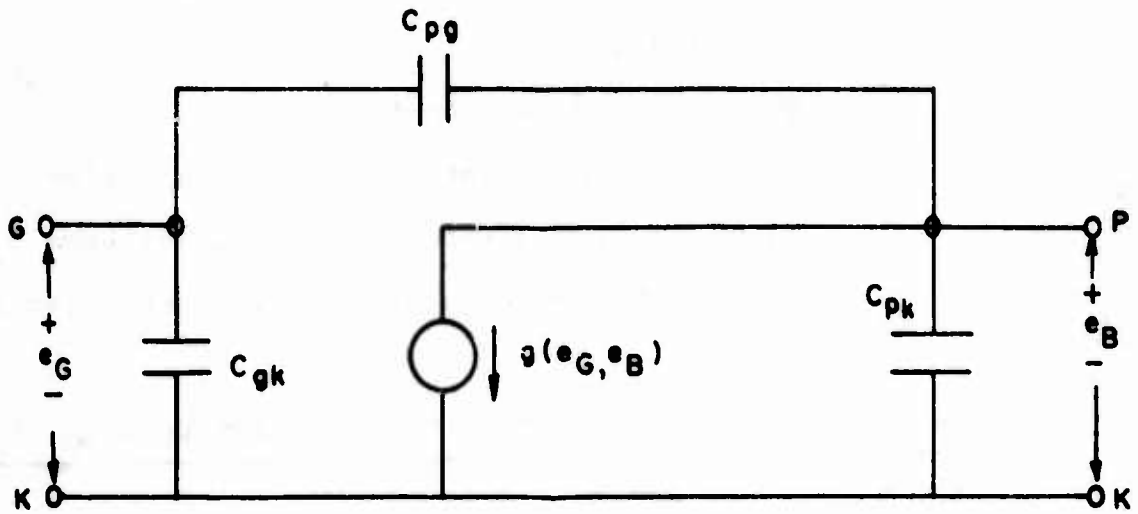

Fig. 3.6-1. Total equivalent circuit for the vacuum tube triode.

The expression for the current $g(e_G, e_B)$ used in NCAP is

$$g(e_G, e_B) = G_o \left[1 - e_G/E_{C_{max}}\right] \left[e_G + \phi + e_B/\mu\right]^{1.5} \quad (3.6\text{-}1)$$

The NCAP model parameters G_o, μ, ϕ, $E_{C_{max}}$, E_G and E_B are defined in Table 3.6-1.

TABLE 3.6-1

NCAP Vacuum Tube Triode Model Parameters

Parameter	Description
E_G	DC grid-cathode voltage at operating point
E_B	DC plate-cathode voltage at operating point
G_o	Perveance for $e_G = 0$
$E_{C_{max}}$	Grid-Cathode voltage for zero perveance
ϕ	Offset voltage
μ	Triode amplification factor
C_{gk}	Grid to Cathode interelectrode capacitance
C_{pg}	Plate to Grid interelectrode capacitance
C_{pk}	Plate to Cathode interelectrode capacitance

3.6.2 Determining the Vacuum Tube Triode Parameters E_G, E_B, G_o, $E_{C_{max}}$, ϕ, and μ

Values for the vacuum tube triode model parameters E_G and E_B are determined from the dc operating point data for the triode. The model parameters G_o, $E_{C_{max}}$, ϕ, and μ are determined from the triode dc plate current I_B vs dc plate-cathode voltage E_B characteristics as a function of the dc grid-cathode voltage E_G. The I_B-E_B triode characteristics are usually provided by vacuum tube manufacturers. If manufacturer's data are not available, the I_B-E_B characteristics can be measured using the experimental system shown in Fig. 3.6-2. Shown in Fig. 3.6-3 are I_B vs E_B characteristics for one section of a 12AT7 dual triode.

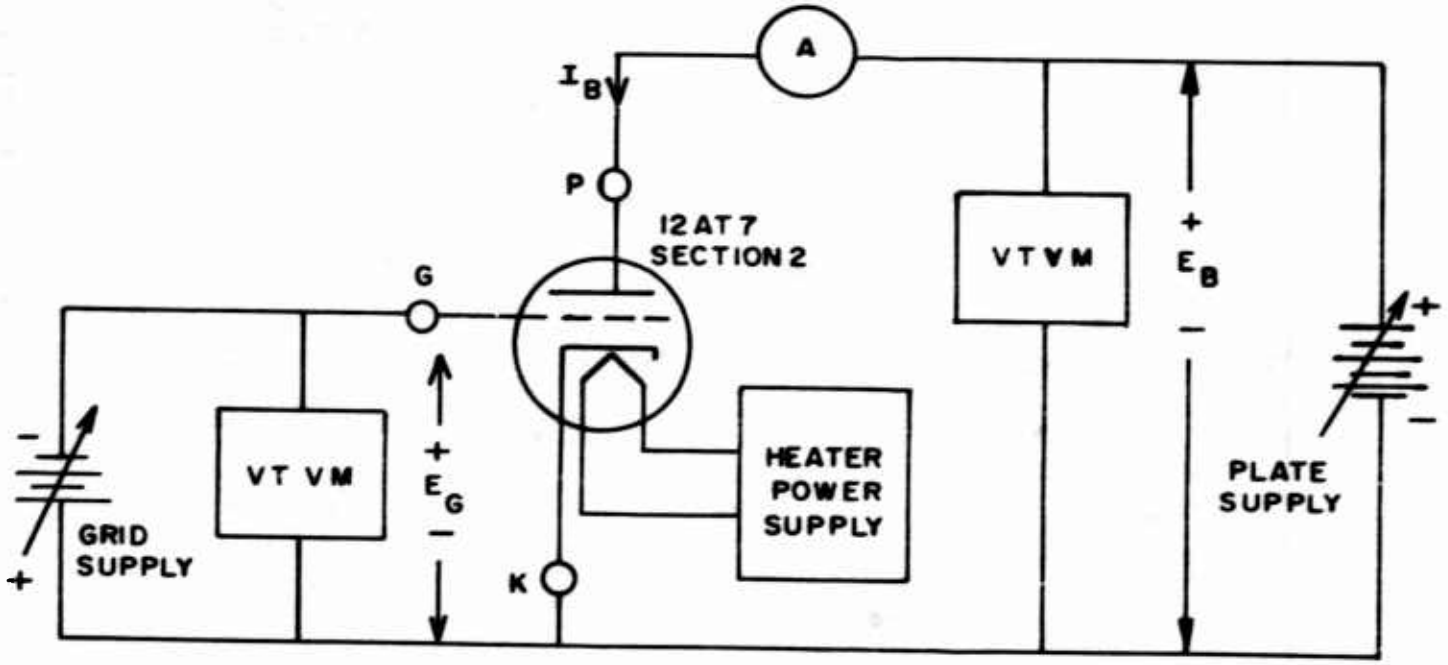

Fig. 3.6-2. Experimental system for measuring the I_B - E_B characteristics of one section of a 12AT7 (dual triode).

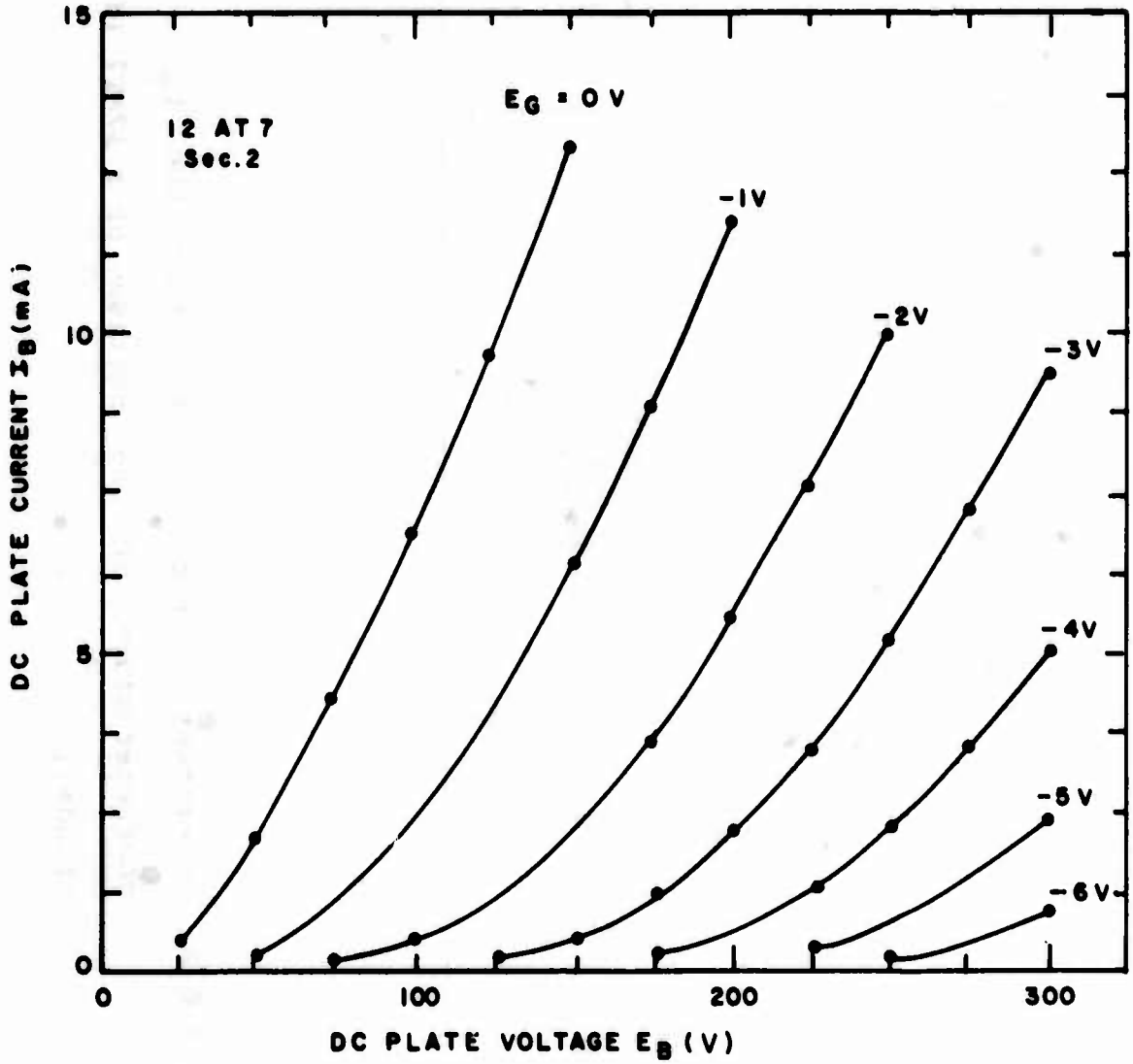

Fig. 3.6-3. DC I_B - E_B characteristics for one section of a 12AT7 triode.

From Eq. (3.6-1) the dc plate current I_B can be written as

$$I_B = G(E_G)\ [E_G + \phi + E_B/\mu]^{1.5} \qquad (3.6\text{-}2)$$

$$G(E_G) = G_o\ [1 - E_G/E_{C_{max}}] \qquad (3.6\text{-}3)$$

where E_G and E_B are the dc grid-cathode and plate-cathode voltages. It is informative to plot values of $I_B^{2/3}$ vs E_B as shown in Fig. 3.6-4. From Eq. (3.6-2) the expression obtained for $I_B^{2/3}$ vs E_B for constant E_G, μ and ϕ is that of a straight line.

$$I_B^{2/3} = [G(E_G)^{2/3}/\mu]\ [\mu E_G + \mu\phi + E_B] \qquad (3.6\text{-}4)$$

For constant E_G, μ, and ϕ the slope $S(E_G)$ and E_B axis intercept $I(E_G)$ from Eq. (3.6-4) are

$$\text{Slope } S(E_G) = G(E_G)^{2/3}/\mu \qquad (3.6\text{-}5)$$

$$\text{Intercept } I(E_G) = -(\mu E_G + \mu\phi) \qquad (3.6\text{-}6)$$

From Fig. 3.6-4 it is seen that the plots of $I_B^{2/3}$ vs E_B are straight lines for values of $I_B^{2/3} > .02\ A^{2/3}$ ($I_B > 2.8$ mA). The slope $S(E_G)$ of the straight line segments are given in Table

3.6-2. If the straight line segments through the values of $I_B^{2/3}$ vs E_B for $I_B^{2/3} > .02\ A^{2/3}$ are extrapolated to $I_B^{2/3} = 0$, the values for the E_B axis intercept $I(E_G)$ given in Table 3.6-2 are obtained. If the value for ϕ is assumed constant, values for μ can be calculated from

$$\mu = \Delta I(E_G) / (-\Delta E_G) \qquad (3.6\text{-}7)$$

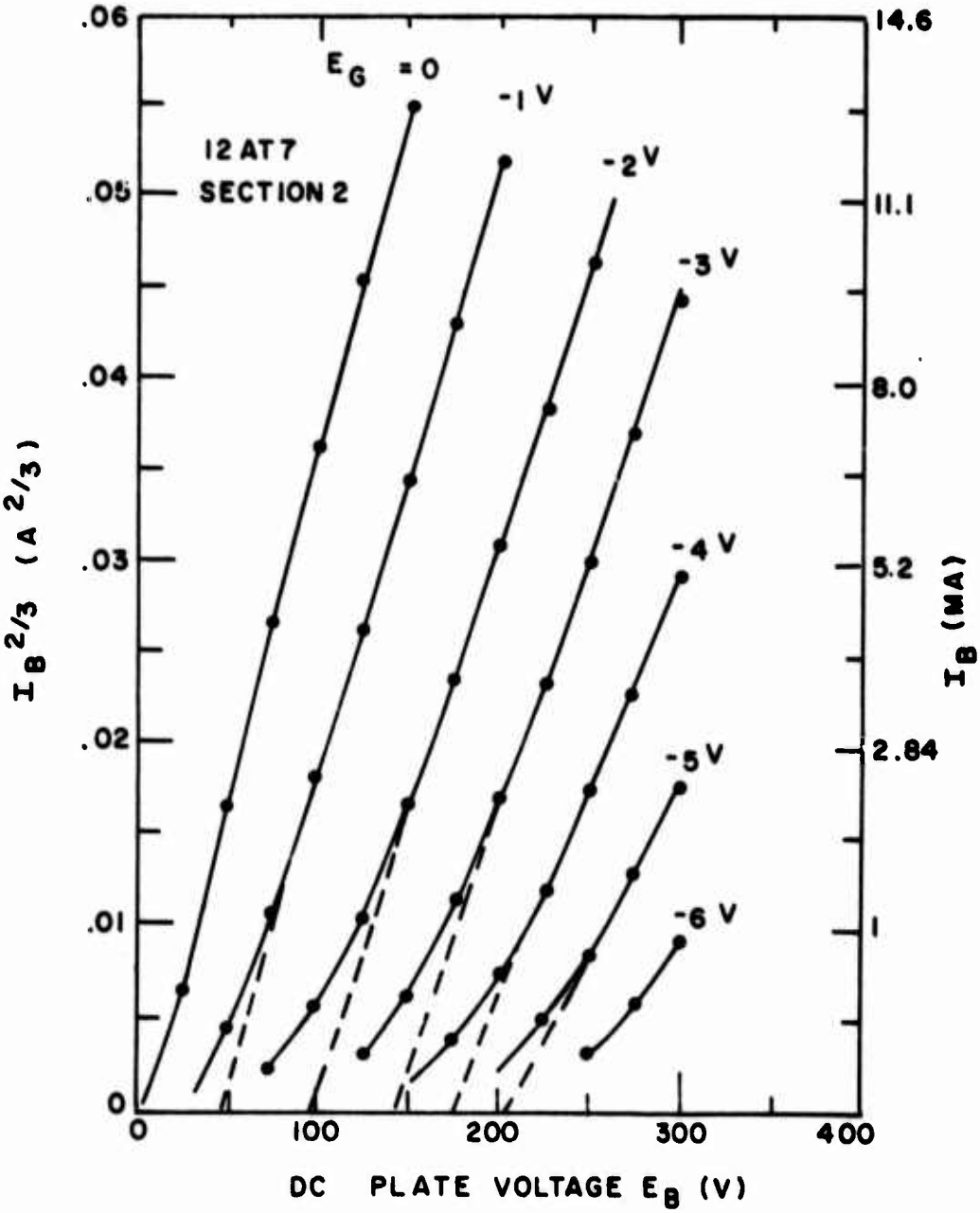

Fig. 3.6-4. Values of $I_B^{2/3}$ vs E_B for one section of a 12AT7 triode.

TABLE 3.6-2

Values of the Slope S, Intercept I, μ, and G as a Function of E_G From $I_B^{2/3}$ vs E_B Data

E_G (V)	Slope S ($A^{2/3}/V$)	Intercept I (V)	μ $\Delta I/-\Delta E_G$	Perveance G in $A/V^{1.5}$ μ = 50	μ = 40	μ = 30
0	.000420	9		.00304	.00218	.00141
0 to -1			36			
-1	.000336	45		.00218	.00156	.00101
-1 to -2			51			
-2	.000306	96		.00189	.00135	.00088
-2 to -3			46			
-3	.000278	142		.00164	.00117	.00076
-3 to -4			31			
-4	.000224	173		.00119	.00085	.00055
-4 to -5			30			
-5	.000186	203		.00090	.00064	.00042

The calculated values for μ for a specific range of E_G values corresponding to ΔE_G are also given in Table 3.6-2. As the grid-cathode dc bias becomes more negative, the values for μ initially increase and then decrease. Since the computer program NCAP uses a constant value for μ, a single value for μ must be chosen. Values for μ=50, 40, and 30 are possible choices.

A value for $E_{C_{max}}$ can be determined using the following procedures. First Eq. (3.6-5) is written in the form

$$G(E_G) = [\mu \cdot \text{slope } S(E_G)]^{1.5} \qquad (3.6\text{-}8)$$

Next using Eq. (3.6-8) and the values for the slope $S(E_G)$ given in Table 3.6-2, values for $G(E_G)$ are calculated for μ values of 50, 40, and 30. (See Table 3.6-2.) The resulting values of $G(E_G)$ vs E_G are plotted as in Fig. 3.6-5. The plots are straight line segments for $E_G \leq -1$ V in agreement with Eq. (3.6-3). By extrapolating the straight lines, values for G_o (G - axis intercept) and $E_{C_{max}}$ (E_G - axis intercept) are obtained. These values are listed in Table 3.6-3.

TABLE 3.6-3

Values of $E_{C_{max}}$ and G_o vs μ For One Section of a 12AT7 Triode

μ	$E_{C_{max}}$ V	G_o $mA/V^{1.5}$
50	-7.9	2.5
40	-7.8	1.8
30	-7.9	1.15

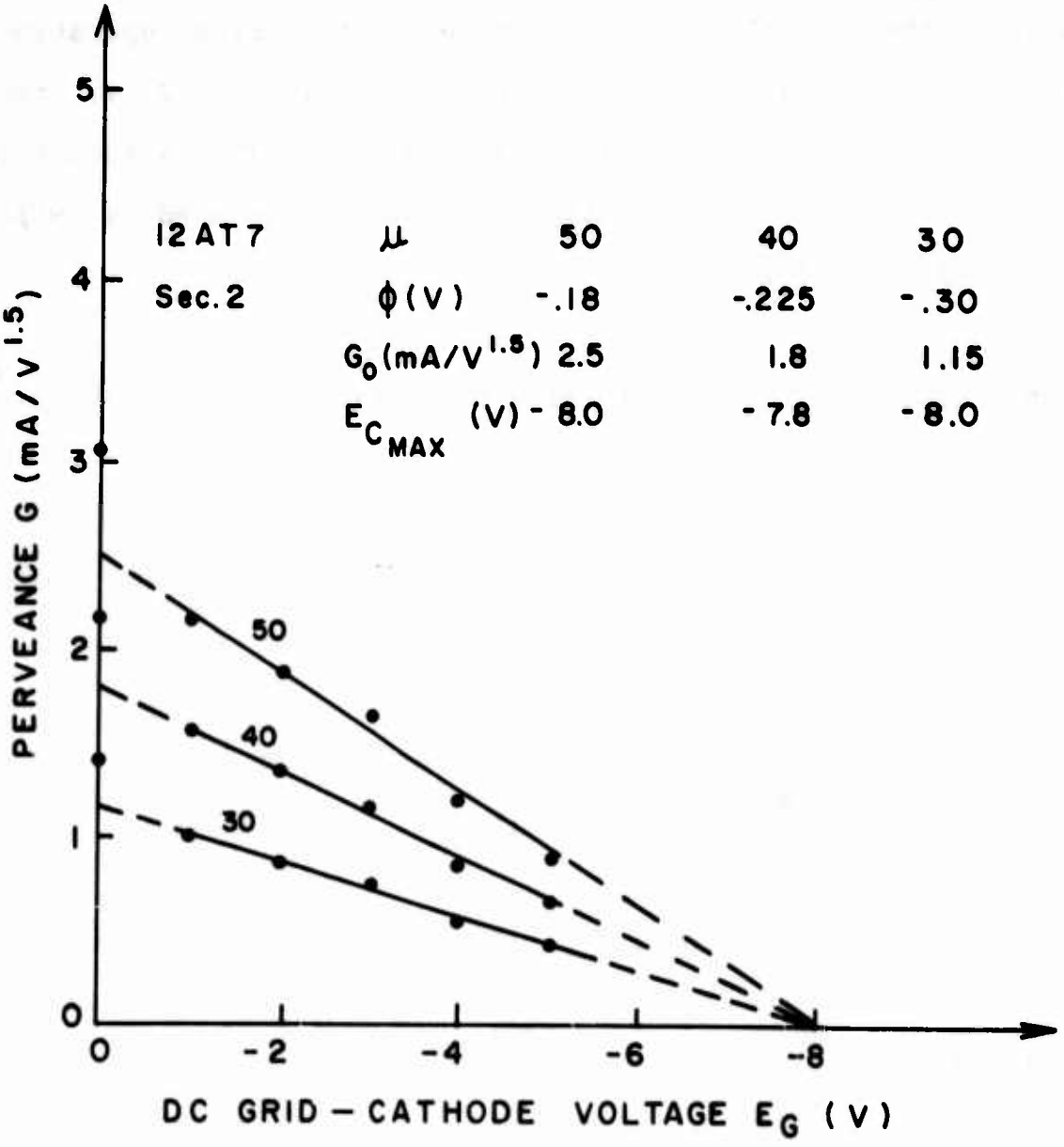

Fig. 3.6-5. Perveance G vs dc grid-cathode voltage E_G. G_o is the G - axis intercept. $E_{C_{max}}$ is the E_G axis intercept.

It is observed that the value for $E_{C_{max}}$ is independent of the value used for μ. However, the value for G_o does depend upon the μ value. The μ value is determined by the triode operating point. For example if E_G is in the range -1 to -2 V, the appropriate value is μ=51. (See Table 3.6-2). Then values for G_o and ϕ corresponding to μ = 51 (or 50) should be used as NCAP triode model parameters.

The procedure for determining NCAP triode model parameters may be summarized as follows:

(1) Determine E_B and E_G from the triode dc operating point data.

(2) Using Table 3.6-2, determine a single value for μ based upon the value for E_G. Interpolate if necessary.

(3) Using Table 3.6-3 and the μ value determined in step (2), determine a value for $E_{C_{max}}$ and G_o. Interpolate if necessary.

(4) Use Eq. (3.6-6) to calculate ϕ. To obtain a value for $I(E_G)$ use the $I(E_G)$ vs E_G data given in Table 3.6-2. Interpolate if necessary.

To illustrate the procedure a specific example is presented. The 12AT7 dc operating point data are assumed to be E_B = +200 V and E_G = -1.5 V. From Table 3.6-2, $\mu \simeq 50$. From Table 3.6-3 $E_{C_{max}}$ = -7.9 V and G_o = .0025 $A/V^{1.5}$. Using Table 3.6-2, the intercept $I(E_G)$ is estimated to be 70 V at E_G = -1.5 V. Using Eq. (3.6-5) with I = 70 V and E_G = -1.5 V, the value ϕ = +.1 V is obtained. (Note that the value obtained is positive.) These ϕ values are summarized in Table 3.6-4.

TABLE 3.6-4

Values of NCAP Model Parameters For One Section of a 12AT7 Triode

E_B = +200 V	$E_{C_{max}}$ = -7.9 V
E_G = -1.5 V	G_o = .0025 $A/V^{1.5}$
μ = 50	ϕ = +.1 V

3.6.3 Determining the Vacuum Tube Triode Parameters C_{gk}, C_{pg}, and C_{pk}

An examination of data provided by manufacturer's of vacuum tube triodes indicates that values for the interelectrode capacitances are usually available. If this is <u>not</u> the case, the interelectrode capacitances can be measured directly on a 1 MHz capacitance bridge using procedures similar to those described in Section 3.5.3 for the vacuum tube diode.

When manufacturer's data are available, their use is recommended. The following interelectrode capacitance data for the 12AT7 twin triode are taken from the RCA Receiving Tube Manual.

Direct Interelectrode Capacitance

	Without External Shield	With External Shield
Grid-Drive Operation	pF	pF
Grid to Plate (Each Unit)	1.5	1.5
Grid to Cathode & Heater (Each Unit)	2.2	2.2
Plate to Cathode and Heater		
Unit No. 1	0.5	1.2
Unit No. 2	0.4	1.5

Based upon the direct interelectrode capacitance data provided, the capacitance values given in Table 3.6-5 were estimated. The values for C_{gk}, C_{pg}, and C_{pk} can be entered directly as NCAP parameter values for the triode. If a shield is used, the plate to shield capacitance C_{ps} can be specified separately as an extrinsic (passive) component. (The shield would usually be at ground potential.) Again it is important to note that other parasitic capacitances such as those associated with the tube socket and leads connected to the tube socket terminals may be

important. Important parasitic capacitances can be specified separately as extrinsic (passive) components.

TABLE 3.6-5

Values For The Interelectrode Capacitances for the 12AT7 Triode

C_{gk} (Both units)	2.2×10^{-12} F
C_{pg} (Both units)	1.5×10^{-12} F
C_{pk} (Unit 1)	0.5×10^{-12} F
C_{pk} (Unit 2)	0.4×10^{-12} F
C_{ps} (unit 1)	0.7×10^{-12} F
C_{ps} (Unit 2)	1.1×10^{-12} F

3.7 Vacuum Tube Pentode

The Nonlinear Circuit Analysis Program NCAP can be used to calculate nonlinear effects in electronic circuits containing vacuum tube pentodes. A schematic for the pentode is shown in Fig. 3.7-1. A pentode is normally operated with the suppressor grid connected to the cathode, and the NCAP pentode model is restricted to this case. In this section procedures for determining the NCAP vacuum tube pentode model parameters will be given.

3.7.1 NCAP Model For the Vacuum Tube Pentode

The nonlinear device model used for the vacuum tube pentode in Fig. 3.7-2 may be called a total equivalent model. The interelectrode capacitors C_{gk}, C_{g1g2}, C_{pg}, C_{g2k}, C_{g2p} and C_{pk} are defined in Table 3.7-1. The pentode space-charge currents $f(e_{G1}, e_{G2}, e_B)$ and $g(e_{G1}, e_{G2}, e_B)$ depend upon the total instantaneous control-grid cathode voltage e_{G1}, total instantaneous screen-grid cathode voltage e_{G2}, and total instantaneous plate cathode voltage e_B. These currents are given by

$$f(e_{G1}, e_{G2}, e_B) = G_0 \left[1 - \frac{e_{G1}}{E_{C_{max}}}\right] \left(e_{G1} + \phi + \frac{e_{G2}}{\mu}\right)^{\frac{3}{2}} \frac{\frac{1}{D}}{\frac{1}{D} + \left(\frac{e_B}{e_{G2}}\right)^m} \qquad (3.7\text{-}1)$$

$$g(e_{G1},e_{G2},e_B) = G_0 \left[1 - \frac{e_{G1}}{E_{C_{max}}}\right] \left(e_{G1} + \phi + \frac{e_{G2}}{\mu}\right)^{\frac{3}{2}} \frac{\left(\frac{e_B}{e_{G2}}\right)^m}{\frac{1}{D} + \left(\frac{e_B}{e_{G2}}\right)^m}$$

(3.7-2)

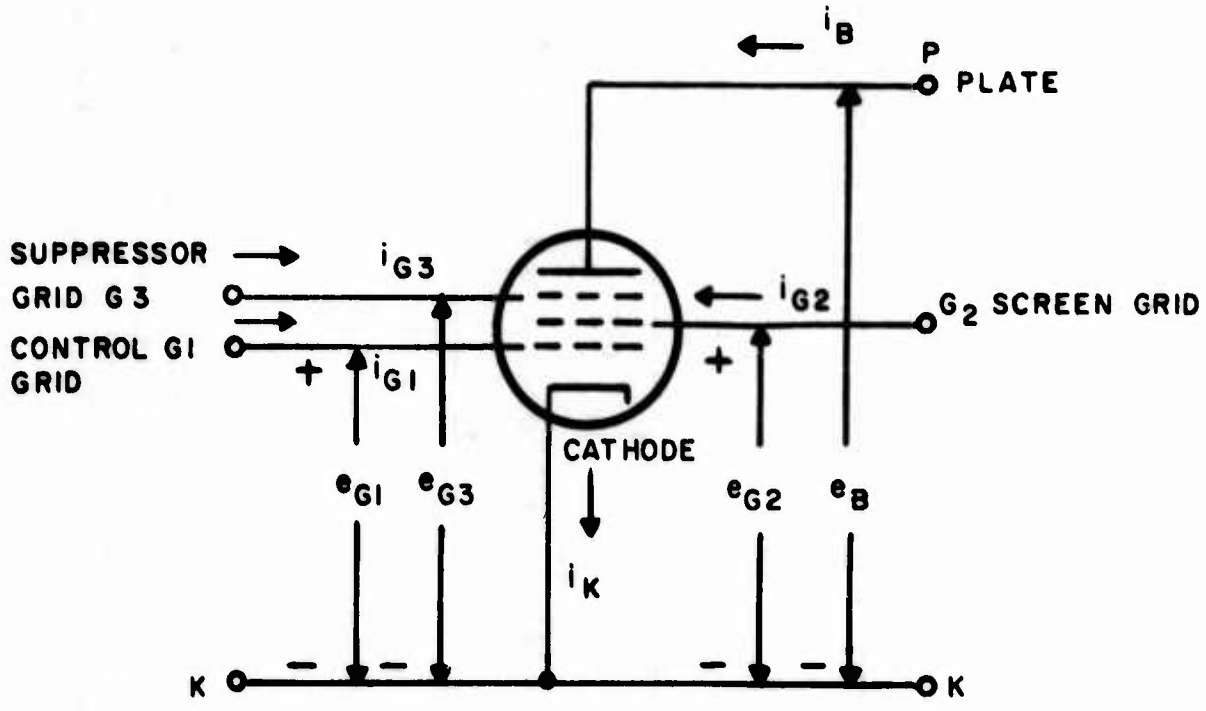

Fig. 3.7-1. Vacuum tube pentode schematic illustrating pentode total instantaneous terminal currents and voltages (with respect to cathode). In normal pentode operation the suppressor grid is connected to the cathode ($e_{G3} = 0$).

The NCAP pentode model parameters G_o, $E_{C_{max}}$, μ, ϕ, E_{G1}, E_{G2}, E_B, D, and m are defined in Table 3.7-1.

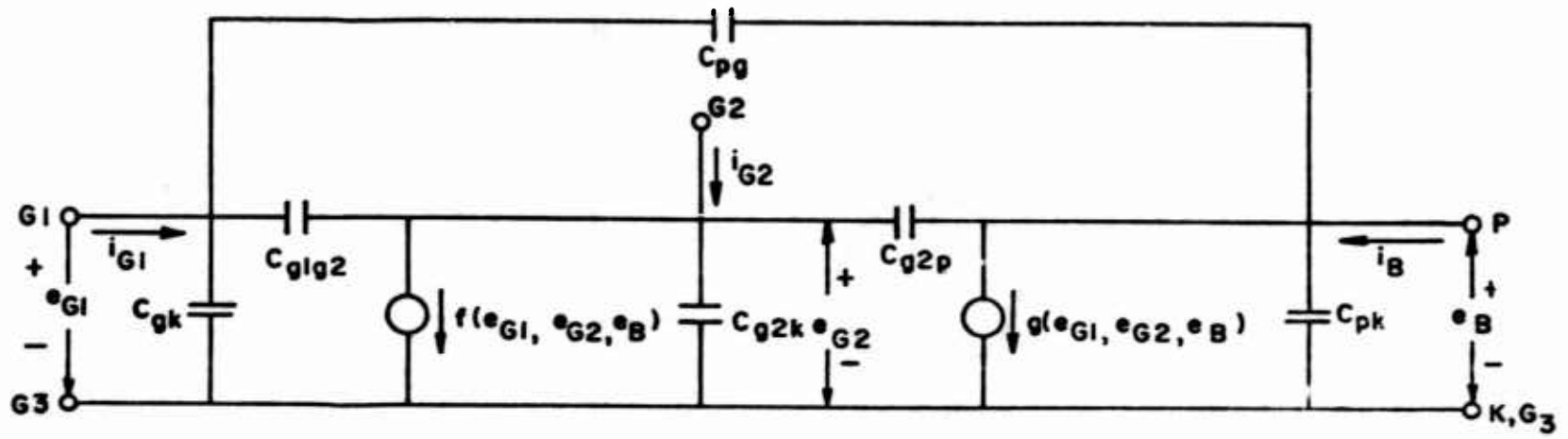

Fig. 3.7-2 Total equivalent circuit for the vacuum tube pentode for the case where the suppressor grid G3 is connected to the cathode. Note that the capacitor C_{gk} is the sum of the control-grid cathode and suppressor-grid cathode interelectrode capacitances and the capcitor C_{pk} is the sum of the plate suppressor-grid and plate cathode interelectrode capacitances.

TABLE 3.7-1

NCAP Vacuum Tube Pentode Model Parameters For the Case Where Suppressor Grid is Connected to Cathode

Parameter	Description
E_{G1}	DC control-grid cathode voltage at operating point
E_{G2}	DC screen-grid cathode voltage at operating point
E_B	DC plate cathode voltage at operating point
G_o	Perveance for $e_{G1} = 0$
$E_{C_{max}}$	Control-grid cathode voltage for zero perveance
ϕ	Offset voltage
μ	Control-grid amplification factor
D	Space-charge current division constant
m	Space-charge current division exponent
C_{pg}	Plate to control-grid interelectrode capacitance
C_{g1g2}	Control-grid to screen-grid interelectrode capacitance
C_{g2k}	Screen-grid to cathode interelectrode capacitance
C_{gk}	Sum of control-grid to cathode interelectrode capacitance C_{g1k} plus control-grid to suppressor-grid interelectrode capacitance C_{g1g3}; $C_{gk} = C_{g1k} + C_{g1g3}$.
C_{pk}	Sum of plate to cathode interelectrode capacitance C'_{pk} plus plate to suppressor-grid interelectrode capacitance C_{pg3}. $C_{pk} = C'_{pk} + C_{pg3}$.
C_{g2p}	Screen-grid to plate interelectrode capacitance

3.7.2 Determining the Vacuum Tube Pentode Parameters E_{G1}, E_{G2}, E_B.

Values for the vacuum tube pentode model parameters E_{G1}, E_{G2}, and E_B are determined from the dc operating point data for the pentode.

3.7.3 Determining the Vacuum Tube Pentode Parameters μ, $E_{C_{max}}$, G_o and ϕ.

By connecting the screen-grid G2 and plate P together, a pentode can be operated as a triode. The model parameters parameters G_o, $E_{C_{max}}$, ϕ, and D can be determined from the $(I_B + I_{G2})$ vs E_B characteristics as a function of the dc control-grid cathode voltage E_{G1} where I_B is the dc plate current, I_{G2} the dc screen-grid current and E_B the dc plate voltage. Often the $(I_B + I_{G2})$ vs E_B characteristics are provided by vacuum tube manufacturers. If manufacturer's data are not available, the $(I_B + I_{G2})$ vs E_B characteristics can be measured with the same experimental system used for measuring triode characteristics shown previously in Fig. 3.6-2. The triode characteristics for the 6AH6 pentode are shown in Fig. 3.7-3. (The plate and screen-grid are connected together and the ammeter A reads $I_B + I_{G2}$ directly.)

Using Eqs. (3.7-1) and (3.7-2) the sum of the dc plate current I_B and dc screen-grid current I_{G2} can be expressed as

$$(I_B + I_{G2}) = G(E_{G1}) \left[E_{G1} + \phi + E_{G2}/\mu\right]^{1.5} \qquad (3.7\text{-}3)$$

$$G(E_{G1}) = G_o \left[1 - E_{G1}/E_{C_{max}} \right] \qquad (3.7\text{-}4)$$

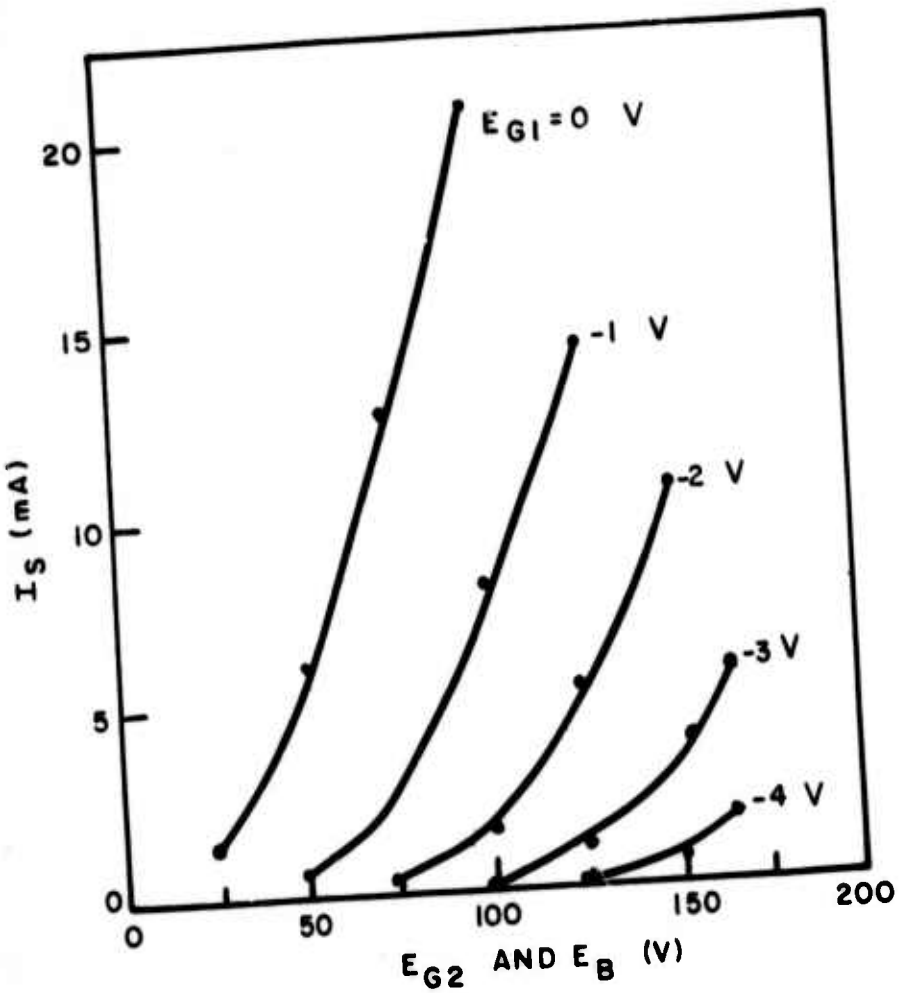

Fig. 3.7-3. Triode characteristics for the 6AH6 pentode.

where E_{G1} and E_{G2} are the dc control-grid cathode and screen-grid

cathode voltages. The next step is to plot values of $(I_B + I_{G2})^{2/3}$ vs E_{G2} as shown in Fig. 3.7-4. From Eq. (3.7-3) the expression for $(I_B + I_{G2})^{2/3}$ obtained is

$$(I_B + I_{G2})^{2/3} = [G(E_{G1})^{2/3}/\mu]\,[\mu E_{G1} + \mu\phi + E_{G2}] \quad (3.7\text{-}5)$$

For a constant E_{G1} value the slope $S(E_{G1})$ and the E_{G2} axis intercept $I(E_{G2})$ of the equation for $(I_B + I_{G2})^{2/3}$ vs E_{G2} are

$$\text{Slope } S(E_{G1}) = G(E_{G1})^{2/3}/\mu \quad (3.7\text{-}6)$$

$$\text{Intercept } I(E_{G1}) = -(\mu E_{G1} + \mu\phi) \quad (3.7\text{-}7)$$

From Fig. 3.7-4 it is seen that the plots of $(I_B + I_{G2})^{2/3}$ vs E_{G2} are straight line segments in agreement with Eq. (3.7-5). The slopes $S(E_{G1})$ determined from the straight line segments are given in Table 3.7-2. If the straight line segments shown in Fig. 3.7-4 are extrapolated to $(I_B + I_{G2})^{2/3} = 0$, the values for the E_{G2} axis intercept $I(E_{G1})$ given in Table 3.7-2 are obtained. If the value for ϕ is assumed constant, values for μ can be calculated from

$$\mu = \Delta I(E_{G1})/(-\Delta E_{G1}) \quad (3.7\text{-}8)$$

The values for the ratio μ calculated using Eq. (3.7-8) for 1 V changes in E_{G1} are also given in Table 3.7-2. The μ values lie

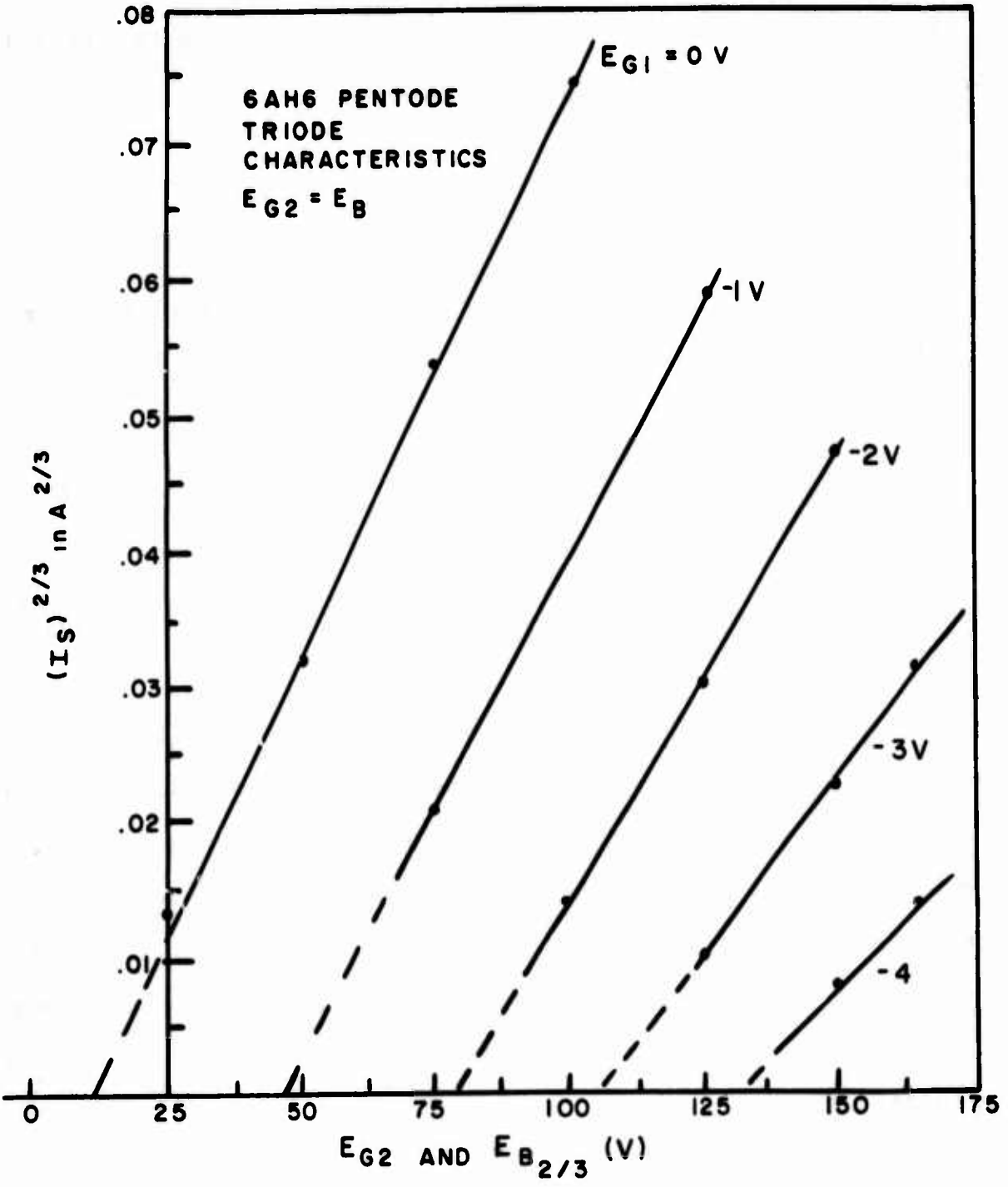

Fig. 3.7-4. Values of $(I_B + I_{G2})^{2/3}$ vs E_{G2} for a triode-connected 6AH6 pentode.

in the range 26 to 34. Since the computer program NCAP uses a constant value for μ, a single value for μ must be chosen. Possible choices for μ are 35, 30 and 25.

TABLE 3.7-2

Values of the Slope $S(E_{G1})$, Intercept $I(E_{G1})$, μ and G As A Function of E_{G1} From $(I_B + I_{G2})^{2/3}$ vs E_B Data For A Triode-Connected 6AH6

E_{G1} (V)	Slope ($A^{2/3}/V$)	Intercept (V)	μ $\Delta I/-\Delta E_G$	Perveance G in $A/V^{1.5}$ $\mu = 35$	$\mu = 30$	$\mu = 25$
0	.000852	12		.00515	.00409	.00311
0 to -1			34			
-1	.000747	46		.00423	.00335	.00255
-1 to -2			33			
-2	.000662	79		.00353	.00280	.00213
-2 to -3			26			
-3	.000514	105		.00241	.00191	.00146
-3 to -4			27			
-4	.000419	132		.00178	.00141	.00107

A value for $E_{C_{max}}$ can be determined using the following procedure. First Eq. (3.7-6) is written as

$$G(E_{G1}) = [\mu \cdot S(E_{G1})]^{1.5} \qquad (3.7\text{-}9)$$

Next using Eq. (3.7-9) and the values for the slope $S(E_{G1})$ given in Table 3.7-2, values for $G(E_{G1})$ are calculated for μ values of 35, 30 and 25. (See Table 3.7-2.) The resulting values of $G(E_{G1})$ vs E_{G1} are plotted in Fig. 3.7-5. The plots are straight line segments in agreement with Eq. (3.7-4). By extrapolating the straight line segments, values for G_o (the $G(E_{G1})$ axis intercept) and $E_{C_{max}}$ (the E_{G1} axis intercept) are determined. These values are listed in Table 3.7-3.

TABLE 3.7-3

Values of $E_{C_{max}}$ and G_o vs μ For a 6AH6 Pentode

μ	$E_{C_{max}}$ (V)	G_o ($mA/V^{1.5}$)
35	-6.1	5.1
30	-6.1	4.1
25	-6.1	3.1

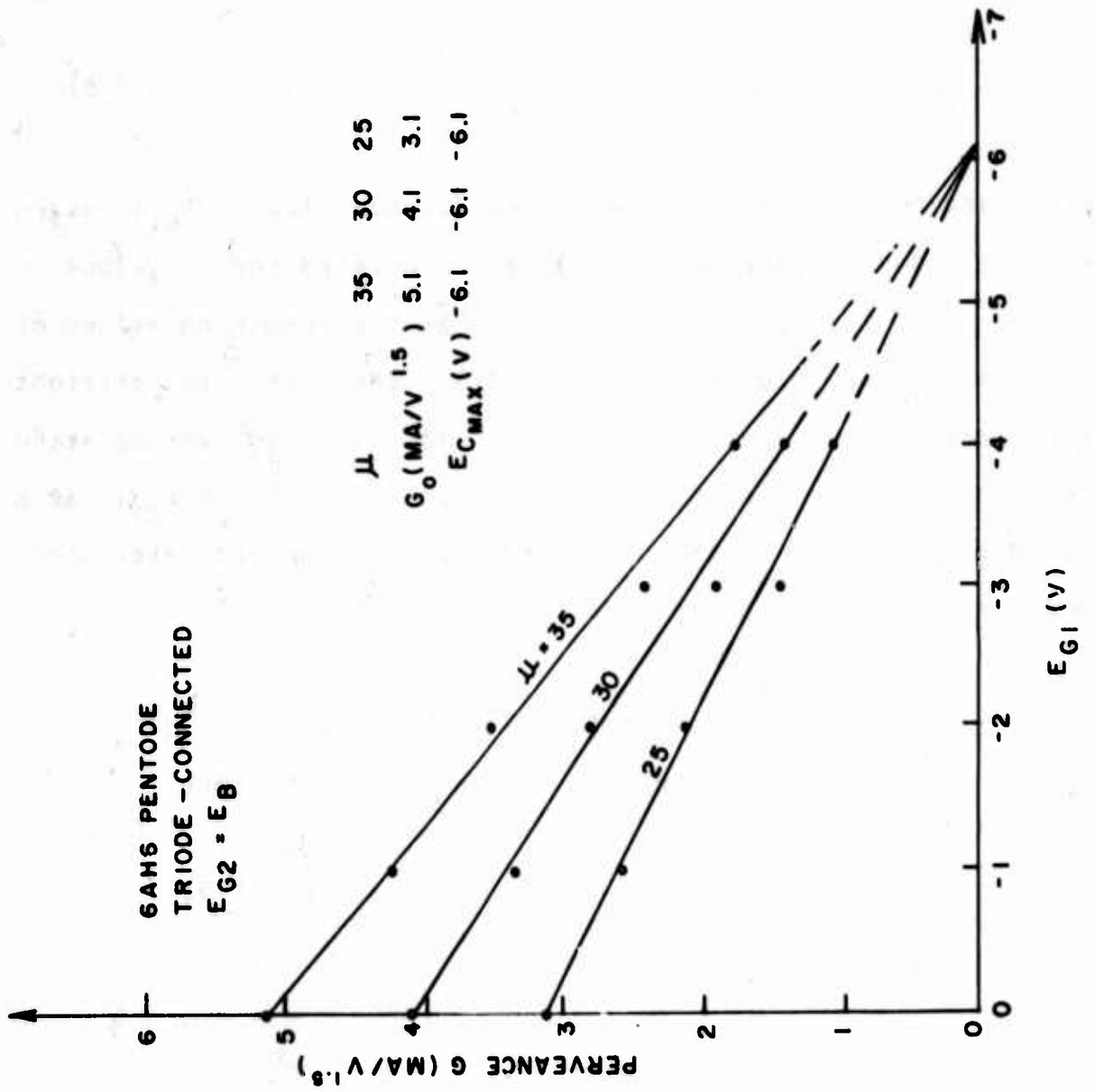

Fig. 3.7-5 Perveance $G(E_{G1})$ vs dc control-grid cathode voltage E_{G1}.

The $E_{C_{max}}$ value is observed to be independent of the value used for μ. However, the value for G_o does depend upon the value used for μ. The value for μ is determined by the pentode operating point.

The following procedure for determining the NCAP pentode model parameters E_{G2}, E_{G1}, G_o, $E_{C_{max}}$, μ, and ϕ is recommended.

(1) Determine E_{G2} and E_{G1} from the pentode operating point data.

(2) Using Table 3.7-2, determine an appropriate value for μ. Interpolate if necessary.

(3) Using Table 3.7-3 and the μ value determined in step (2), determine the values for $E_{C_{max}}$ and G_o. Interpolate if necessary.

(4) Use Eq. (3.7-7) to calculate $\phi = -I/\mu - E_{G1}$. To obtain a value for $I(E_{G1})$ use the $I(E_{G1})$ vs E_{G1} data given in Table 3.7-2. Interpolate if necessary.

To illustrate the procedure a specific example is presented. The 6AH6 pentode dc operating point data are assumed to be E_{G2} = +150 V and E_{G1} = -2 V. From Table 3.7-2, an appropriate value

for μ is 30. From Table 3.7-3, the values for $E_{C_{max}}$ and G_o at $\mu = 30$ are $E_{C_{max}} = -6.1$ V and $G_o = .0041$ A/V$^{1.5}$. From Table 3.7-2, the intercept $I(E_G)$ is 79 V at $E_{G1} = -2$ V. Using Eq. (3.7-7) with $E_{G1} = -2$ V, $\mu = 30$, $I = 79$ V, the value $\phi = -I/\mu - E_{G1} = -.33$ V is obtained. The NCAP pentode model parameters determined in this subsection are summarized in Table 3.7-4.

TABLE 3.7-4

Values of NCAP Pentode Model Parameters E_{G2}, E_{G1}, μ, $E_{C_{max}}$, G_o, and ϕ for a 6AH6 Pentode

$E_{G2} = +150$ V	$E_{C_{max}} = -6.1$ V
$E_{G1} = -2$ V	$G_o = .0041$ A/V$^{1.5}$
$\mu = 50$	$\phi = -.33$ V

3.7.4 Determining the Vacuum Tube Pentode Parameters D and m

By operating a pentode in conventional manner with suppressor grid G3 connected directly to the cathode K, the pentode parameters D and m can be determined. Using Eqs. (3.7-1) and (3.7-2) the ratio of the dc plate current I_B to the dc screen-grid current I_{G2} can be expressed as

$$I_B/I_{G2} = D[E_b/E_{G2}]^m \qquad (3.7\text{-}10)$$

where E_B is the dc plate cathode voltage and E_{G2} is the dc screen-grid cathode voltage. By measuring the dc currents I_B and I_{G2} for several combinations of the dc voltages E_B and E_{G2} values of the ratio I_B/I_{G2} can be determined. Shown in Fig. 3.7-6 is a logarithmic plot of the dc current ratio I_B/I_{G2} vs the dc voltage ratio E_B/E_{G2} for $.5 \leq E_B/E_{G2} \leq 3$ for several values of the dc control-grid voltage E_{G1}. Ideally the logarithmic plots of I_B/I_{G2} vs E_B/E_{G2} should be straight lines which are independent of E_{G1} but a weak dependence on E_{G1} is observed. The slope of the $\log[I_B/I_{G2}]$ vs $\log[E_B/E_{G2}]$ straight line segment yields a value for m for each value of E_{G1}. The value of I_B/I_{G2} at $E_B/E_{G2} = 1$ yields a value for D for each value of E_{G1}. The values of m and D for several values of E_{G1} are given in Table 3.7-5.

TABLE 3.7-5

Values of m and D for a 6AH6 Pentode

E_{G1} (V)	m	D
-.5	.09	4.0
-1	.11	3.8
-2	.13	3.3
-3	.15	3.0

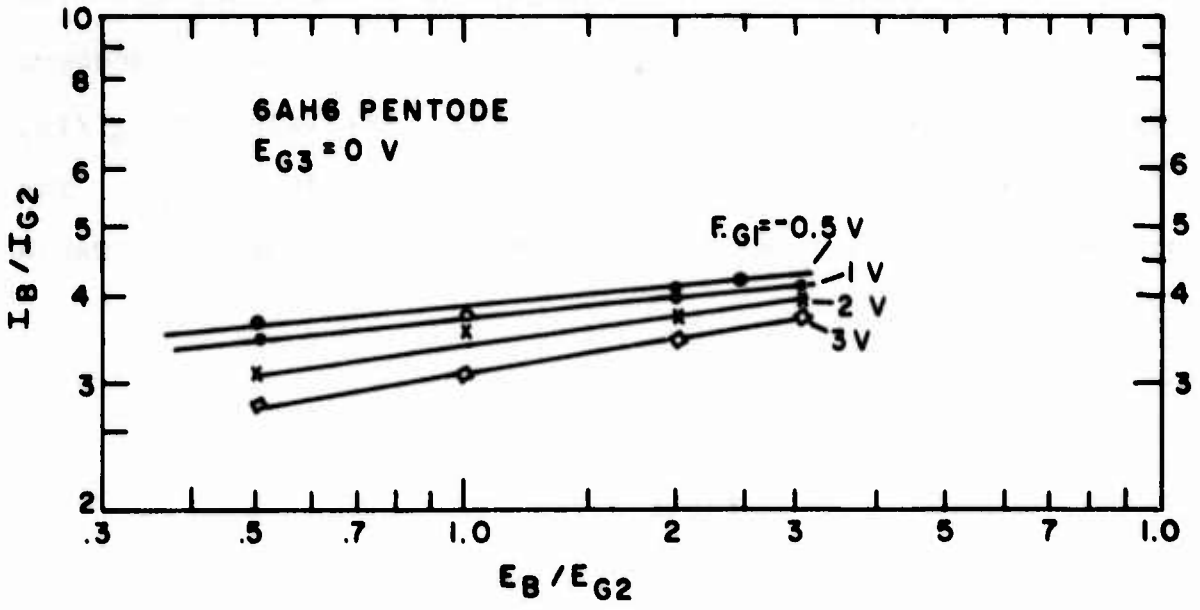

Fig. 3.7-6. Values of the dc current ratio I_B/I_{G2} vs E_B/E_{G2} for several values of the control-grid cathode voltage E_{G1} for a 6AH6 pentode. The suppressor-grid is connected to the cathode.

The following procedure for determining the NCAP pentode model parameters m and D is recommended.

(1) Determine the appropriate value for the control-grid voltage E_{G1} from the dc operating point data.

(2) Use Table 3.7-5 to obtain values for m and D. Interpolate if necessary.

3.7.5 Determining the Vacuum Tube Pentode Interelectrode Capacitances

An examination of data provided by manufacturers of vacuum tube pentodes indicates that values for the major interelectrode capacitances are usually available. If this is not the case or if additional data are needed, the interelectrode capacitances can be measured directly on a 1 MHz capacitance bridge using procedures similar to these described in Section 3.5.3 for the vacuum tube diode.

Interelectrode capacitance data for pentodes are usually provided by manufacturers in the following format.

Direct Interelectrode Capacitances (Approx.)*

Grid No. 1 to Plate	.02 pF
Grid No. 1 to Cathode, Heater, Grid No. 2 Grid No. 3 and Internal Shield	12 pF
Plate to Cathode, Heater, Grid No. 2, Grid No. 3 and Internal Shield	4.7 pF

* External shield connected to cathode

Using the direct interelectrode capacitance data given above, the values C_{pg1} = .02 pf, C_{gk} = 12 pF and C_{pk} = 4.7 pF are obtained. The values for C_{gk}, C_{pk} and C_{pg} can be entered directly as NCAP parameter values for the pentode. Other interelectrode capacitance values, if needed, such as C_{g1g2}, C_{g2k} and C_{g2p} would have to be determined experimentally and specified separately as extrinsic (passive) components.

3.7.6 Summary of Pentode Parameter Values

In Table 3.7-6 the NCAP pentode parameter values for a 6AM6 pentode are given for a specific dc operating point·

E_{G1} = -2 V, E_{G2} = 150 V, and E_B = 300 V.

TABLE 3.7-6

NCAP Parameter Values For a 6AH6 Pentode At A Specific Operating Point (E_{G1} = -2 V, E_{G2} = 150 V, and E_B = 300 V)

Parameter No.	Parameter Name	Value	Units
1	G_o	.0041	$A/V^{1.5}$
2	μ	50	
3	D	3.3	
4	m	.13	
5	E_{G1}	-2	V
6	$E_{C_{max}}$	-6.1	V
7	ϕ	-.33	V
8	E_{G2}	150	V
9	E_B	300	V
10	C_{gk}	12×10^{-12}	F
11	C_{pg}	$.02 \times 10^{-12}$	F
12	C_{pk}	4.7×10^{-12}	F

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